Digital Coil Protection System - Background

- Operating envelope of NSTX_CSU significantly greater than that of NSTX
- Expansion due to increased magnetic field strength (coil currents), changes to device geometry, new coils systems, increased pulse length, and new operating scenarios
- Combined range of currents can result in forces, temperatures, and stresses to both coils and structures that significantly exceed NSTX design limits
- Access to full operating space would result in compromised structural integrity and in some cases catastrophic failure
- Mechanical solution is not feasible (complicated design, cost, schedule, and flexibility)
- Static methods could result in severe operation limitations (e.g., PF4-PF5 simultaneous operation)

Digital Coil Protection System - Background

- Project is determining critical set of values (forces, stresses, temperatures, combinations) that combined with their derivatives define the machine "state" with respect to machine integrity
- Real-time machine integrity determination and protection utilizing fast digital system
- State continuously calculated on high-speed digital computer system and compared to pre-defined limits (like ISTP-001)
- Calculation interval similar to power supply response time (O(ms))
- Protects via interface to Level 1 fault system
- Design in excess computing capacity for future expansion (DCPS → MPS)

Digital Coil Protection System - Requirements

- DCPS will be fail-safe (SIL level hardware, redundancy)
- DCPS will be easily reconfigurable via software (algorithms, state variables, and interlock values)
- The set of limiting values and their derivatives define a “safe operating area” for the device. At any instant in time, the job of the DCPS is to ensure the integrity of the NSTX CSU mechanical structures via the following actions

  1. Determine if any calculated value exceeds operating limit (initiate fault)
  2. Determine if a power supply fault would result in conditions causing DCPS fault (initiate fault)
  3. Determine if (given power supply response, present trajectory, etc.) any DCPS limit would be breached prior to next calculation time (initiate fault)
  4. Predict a future time when it would be possible to attempt a plasma shot with a specified set of coil current envelopes

Digital Coil Protection System - Requirements

5. Determine a set of coil current envelopes allowable for a plasma attempt “right now

6. Compute and archive other quantities that over time can affect machine integrity because of fatigue

7. Evaluate acceptability of potential operating scenarios (static and transient) for a given DCPS configuration

Digital Coil Protection System - Advantages

- Easy reconfiguration – the DCPS algorithms and interlock limits can be easily changed in response to changing experimental requirements or changes in the state of the protected hardware

- The DCPS is capable of monitoring and interlocking a set intersecting/competing objectives with both unmatched accuracy and redundancy

- The DCPS algorithms can be exercised off-line for both post shot evaluative analysis and for scenario development

- DCPS algorithms can provide data to other processes (psc, psrtc, etc.) that can be used to modify process behavior for fault and/or disruption avoidance

- Algorithms can be easily added for new hardware

- Self-check algorithms can continuously monitor system health

Digital Coil Protection System - Requirements

- DCPS will provide real-time protection to NSTX_CSU mechanical components
- DCPS algorithms will protect not only in the instantaneous but also in the "first derivative" sense
- The DCPS will not allow successive plasma attempts at a rate that exceeds the basic duty cycle of the NSTX_CSU (5 s / 1200 s = 0.4 %) (Operation at increased duty cycles may be allowed if either a mechanical means is employed to achieve uniform cooling or algorithms are approved that safely account for the non-uniform cooling effect)
- The hardware and software must be capable of providing simultaneous protection on multiple timescales (coils-power-supplies control systems, forces, stresses and strains, thermal processes)
- Computing hardware shall be chosen with headroom for expansion
- Operation of the DCPS shall be fail safe. It will be impossible to run the machine with the DCPS faulted or in a powered off state
- The DCPS will, where reasonable, use "off the shelf" industry standard components

Digital Coil Protection System - Requirements

- The DCPS will use redundancy, to the greatest extent possible, to increase reliability
- Any fault or failure on any DCPS unit will be considered genuine and cause a Level 1 fault
- Software shall be written in modern, structured programming language
- The DCPS software will include data archive and restore functionality
- The DCPS will be located indoors within a temperature controlled environment (heating and air conditioning) with a maximum ambient temperature of 24 ºC (FCPC junction area)

Digital Coil Protection System - Inputs

Initially each DCPS unit will support 64 analog and up to 96 digital input/output channels

- Analog signals – currents, coolant flows, temperatures, pressures
- Digital signals – status bits from other systems
- All inputs will have over/under-voltage protection
- All inputs will be isolated from the DCPS (e.g., opto-coupler)
- Digital Inputs: 5 V (TTL) or 10 – 32 V (high noise immunity)
- Analog Inputs: ±10 V
  - 5 kHz anti-aliasing filter
  - cable fault detection
- Reset Input: digital input
  - local pushbutton or remote electrical signal
  - fault has precedence

Digital Coil Protection System - Outputs

Currently only envision using one latched fault output fault signal per unit

All outputs will utilize optical isolation to the outside world (e.g., opto-coupler)

Faults: The DCPS will generate a fault if

- A protection interlock level is breached or will be breached prior to the next DCPS calculation time

- The combination of coil currents and temperatures are such that a power supply fault would move the system to a state corresponding to a DCPS faulted state

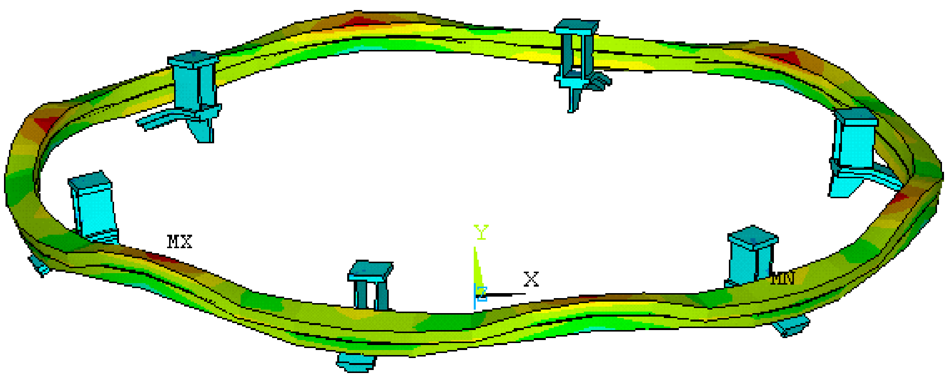
- Internal DCPS system integrity routines determine that there is a problem with the input data

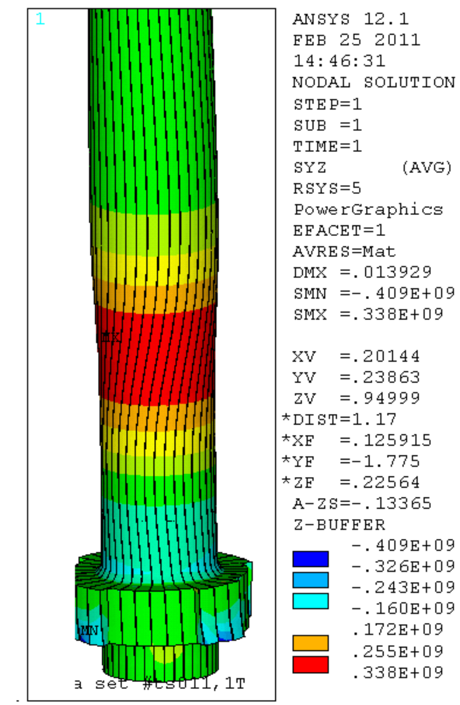
- Internal DCPS self-check routines determine that program or internal data structures are corrupted

- Internal watchdog timer failure

- External watchdog timer failure

NSTX Centerstack Upgrade
Examples of DCPS Input
P. Titus





STRESS MULTIPLIERS FOR THE NSTX UPGRADE DIGITAL COIL PROTECTION SYSTEM

Two approaches are used to provide the needed multipliers/algorithms.

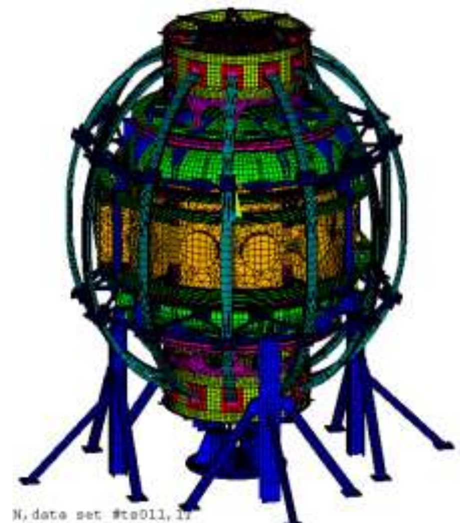
The first is to use the loads on PF coils computed by the DCPS software and apply these to local models of components.

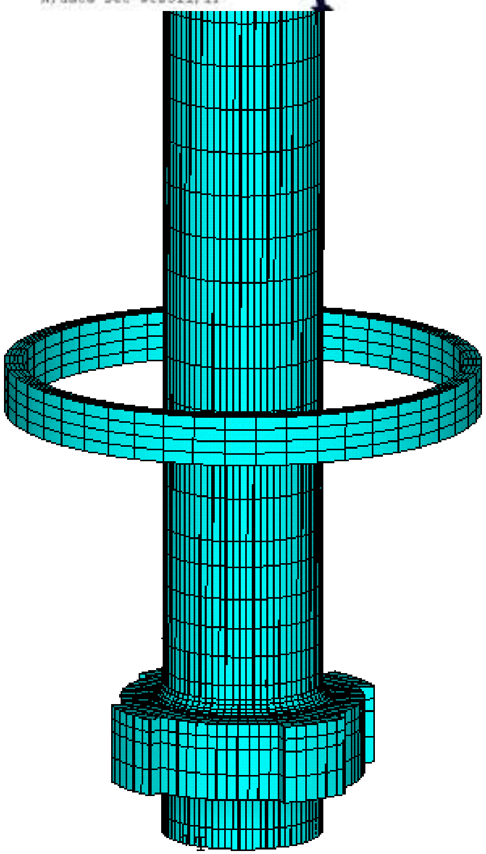
The second approach to calculating the stress multipliers/algorithms is to utilize a global model that simulates the whole structure and includes an adequately refined modeling of the component in question.

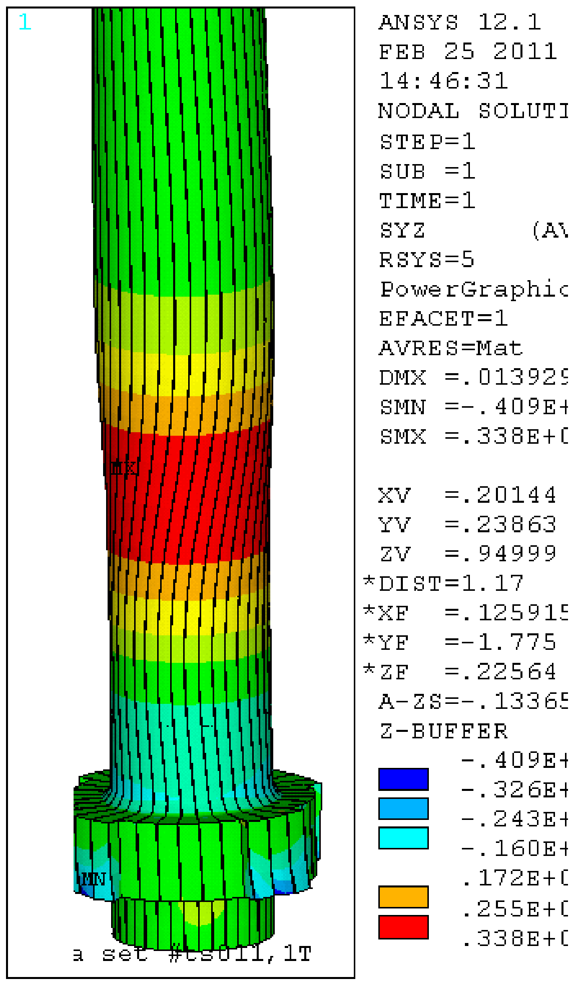
Unit terminal currents are applied to each coil separately, Lorentz loads are calculated, and the response of the whole tokamak and local component stress is computed.

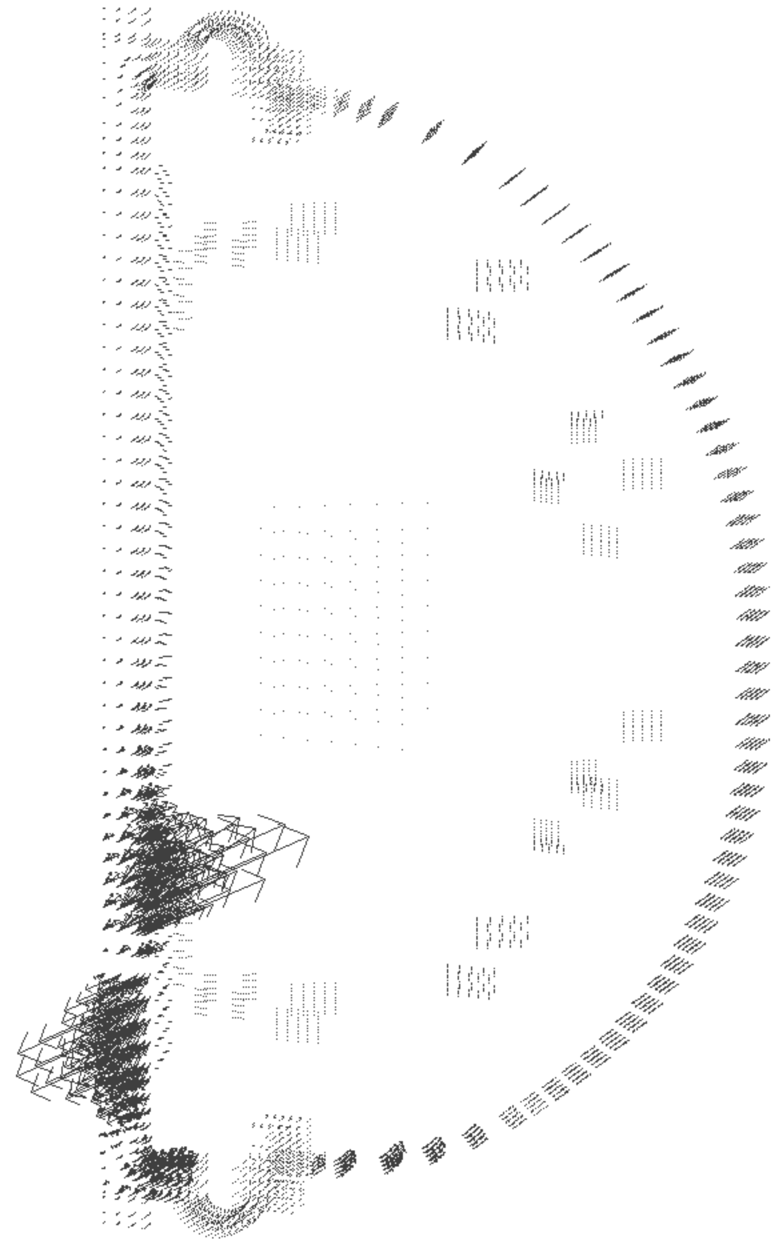
Local component stresses may then be computed in the DCPS or in a spreadsheet for the many scenarios required by the GRD.

PF1CL TF Shear Influence Coefficient Calculation

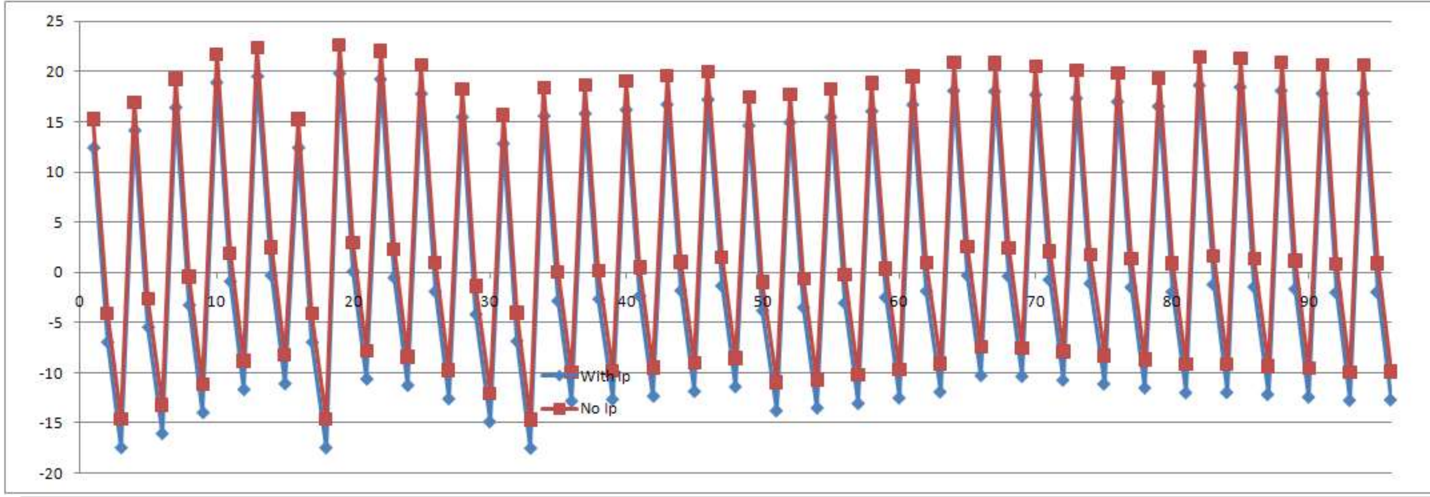




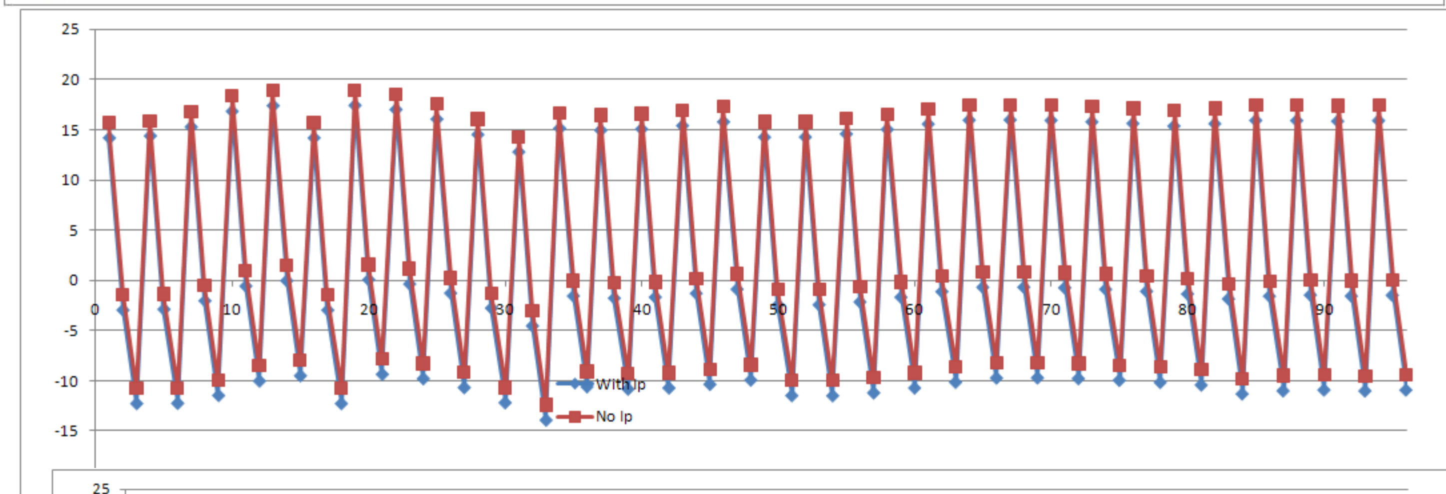




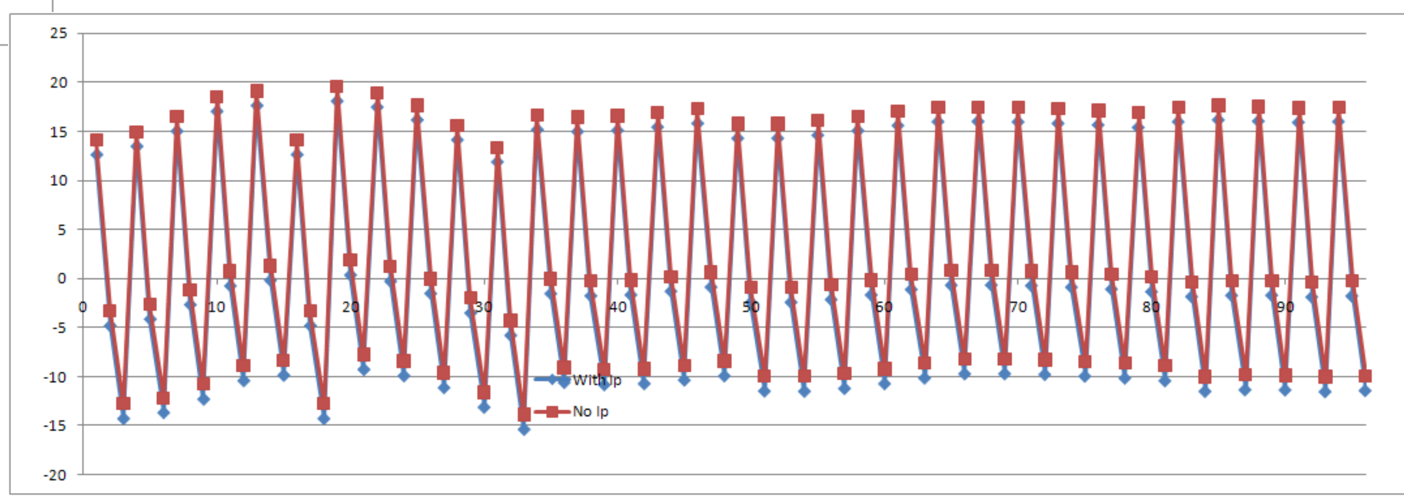
Upper



Upper



Lower

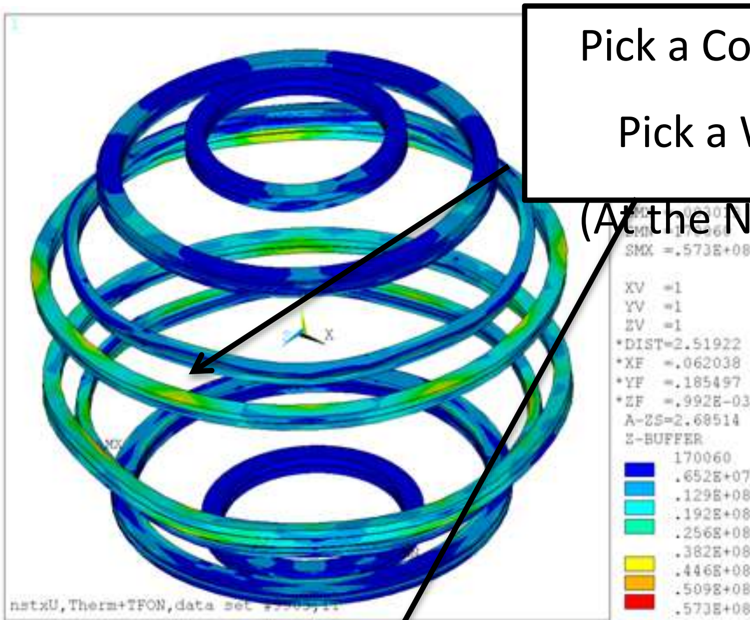


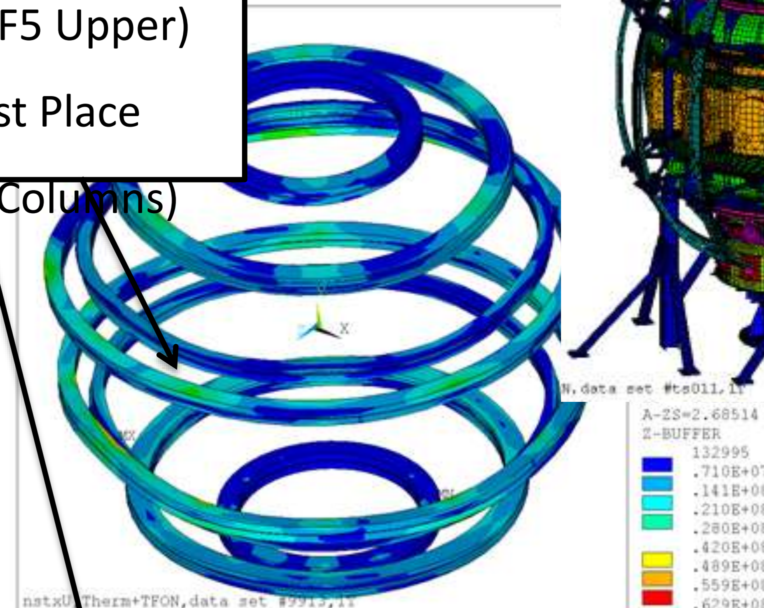
PF5 Upper Coil DCPS Input

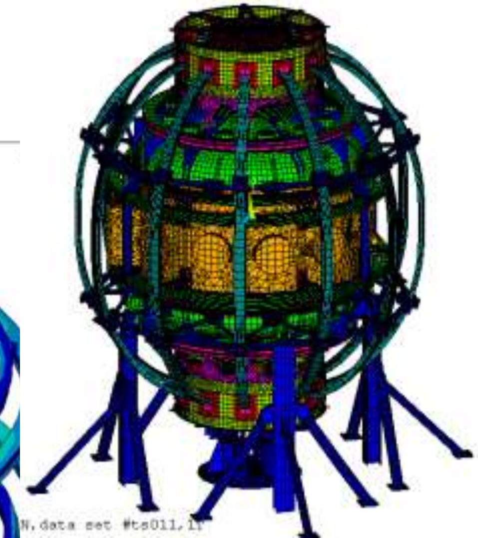
Pick a Coil (PF5 Upper)

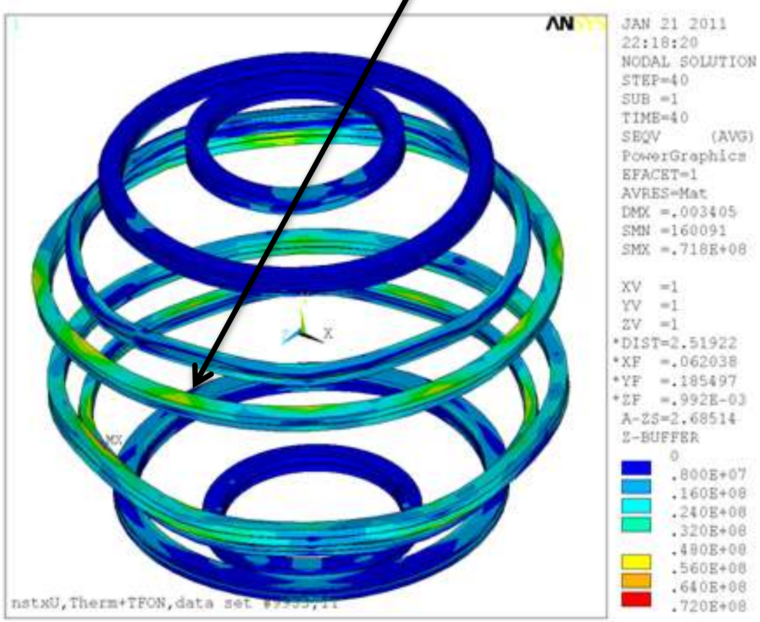
Pick a Worst Place

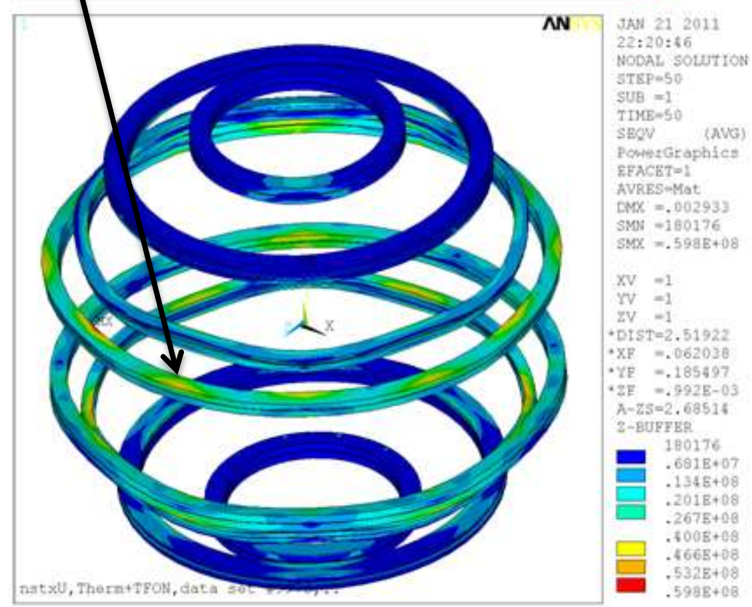
(At the New Columns)



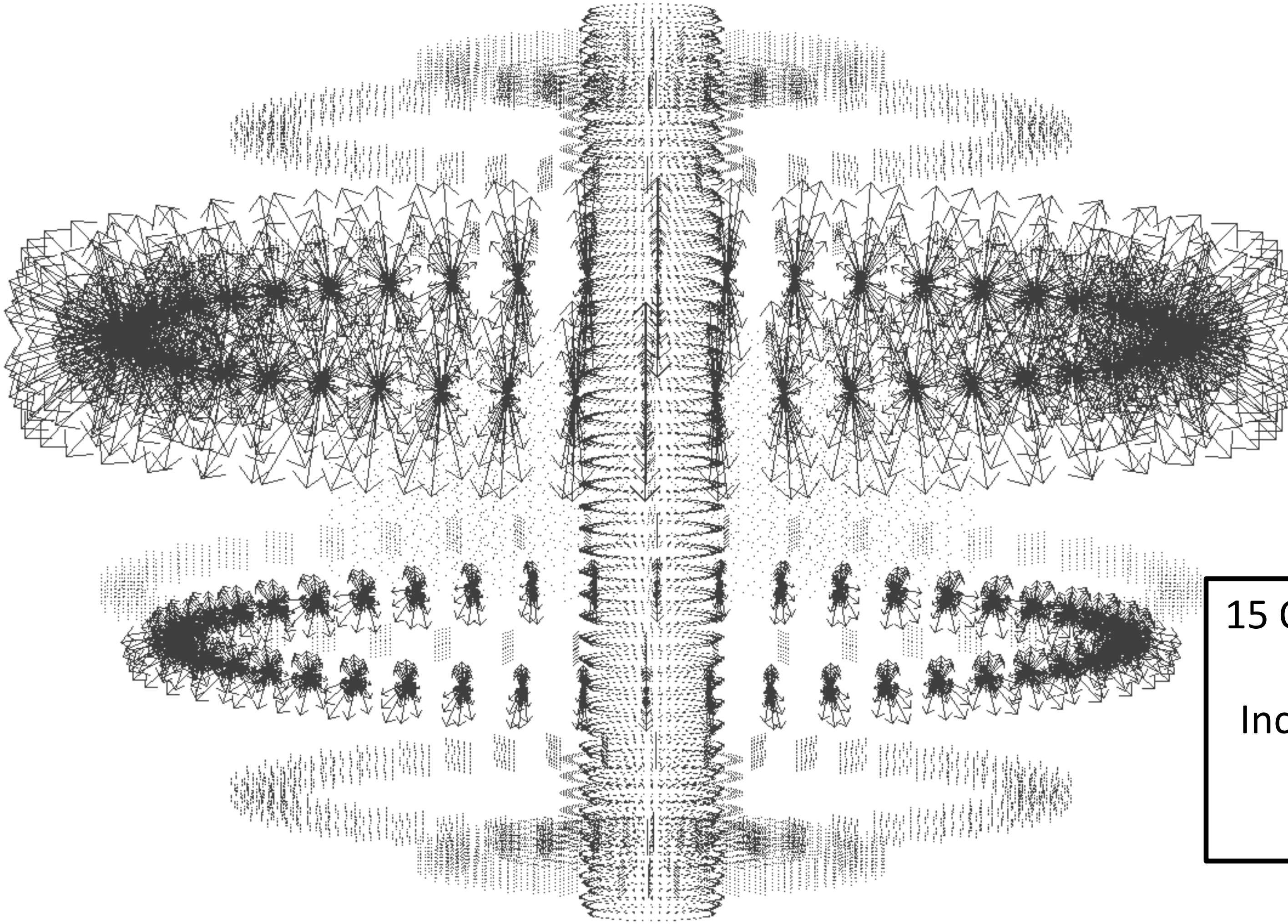




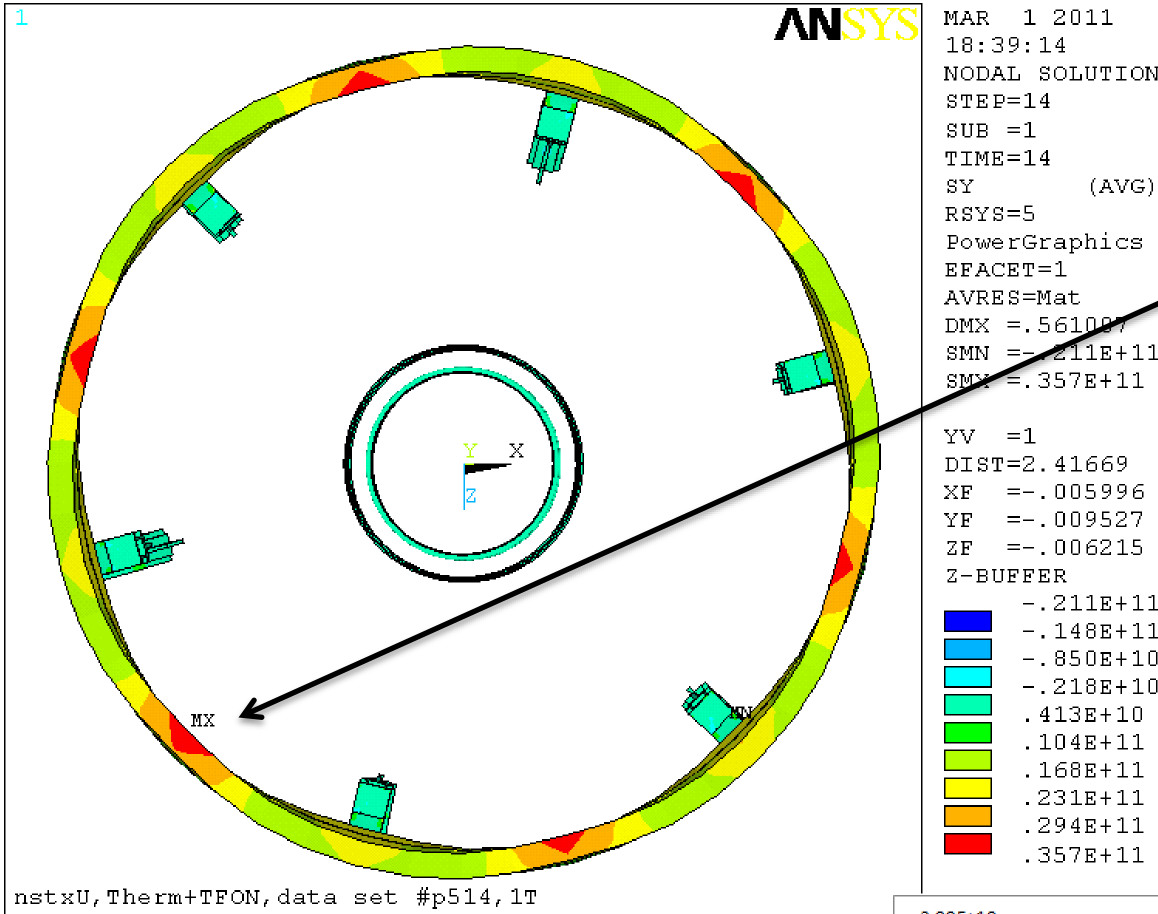




Forces on PF5 (and 4) due to Unit Terminal Currents (actually 1000A) in PF 4 and 5

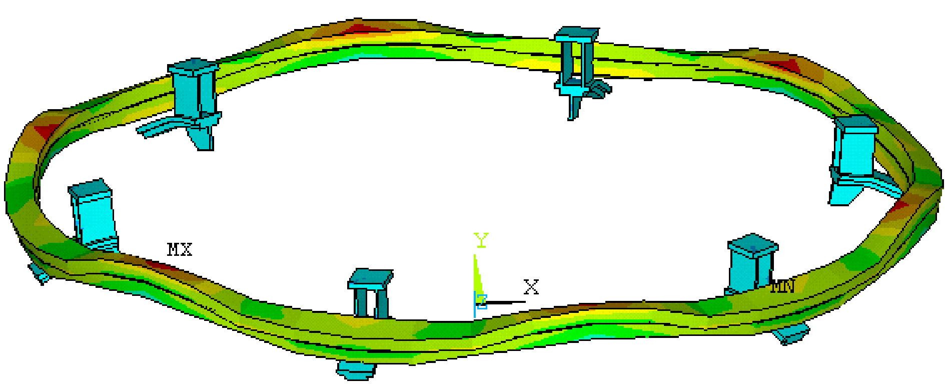


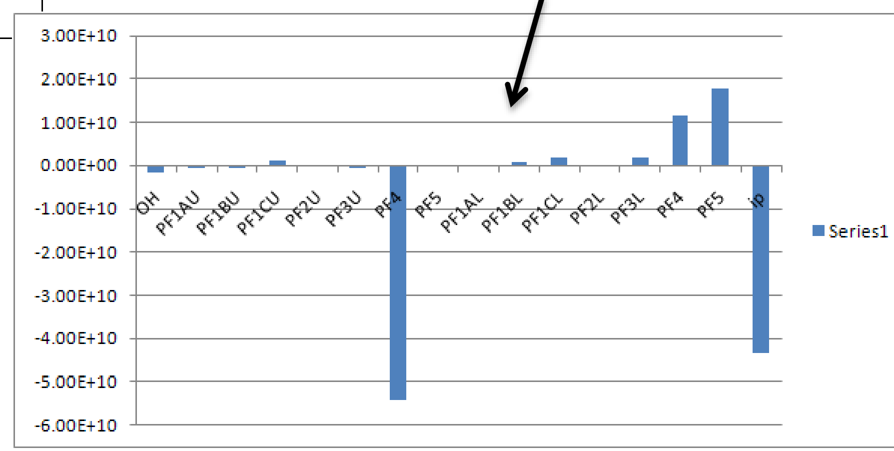
15 Other Sets of Loads Are Calculated, Including one for the Plasma

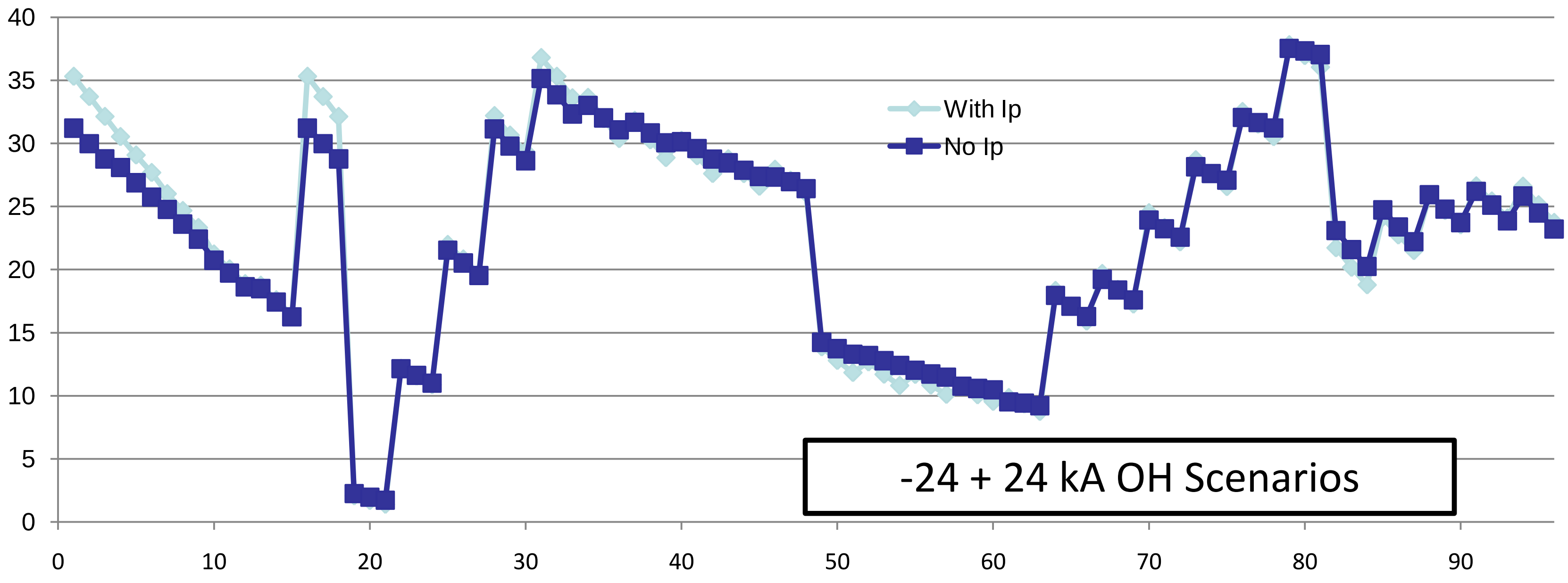


Calculated Influence Coefficient, Load #14 – Stress Due to PF14 Lower

Calculated Influence Coefficients With the PF5 Self Coefficient Subtracted Out







40
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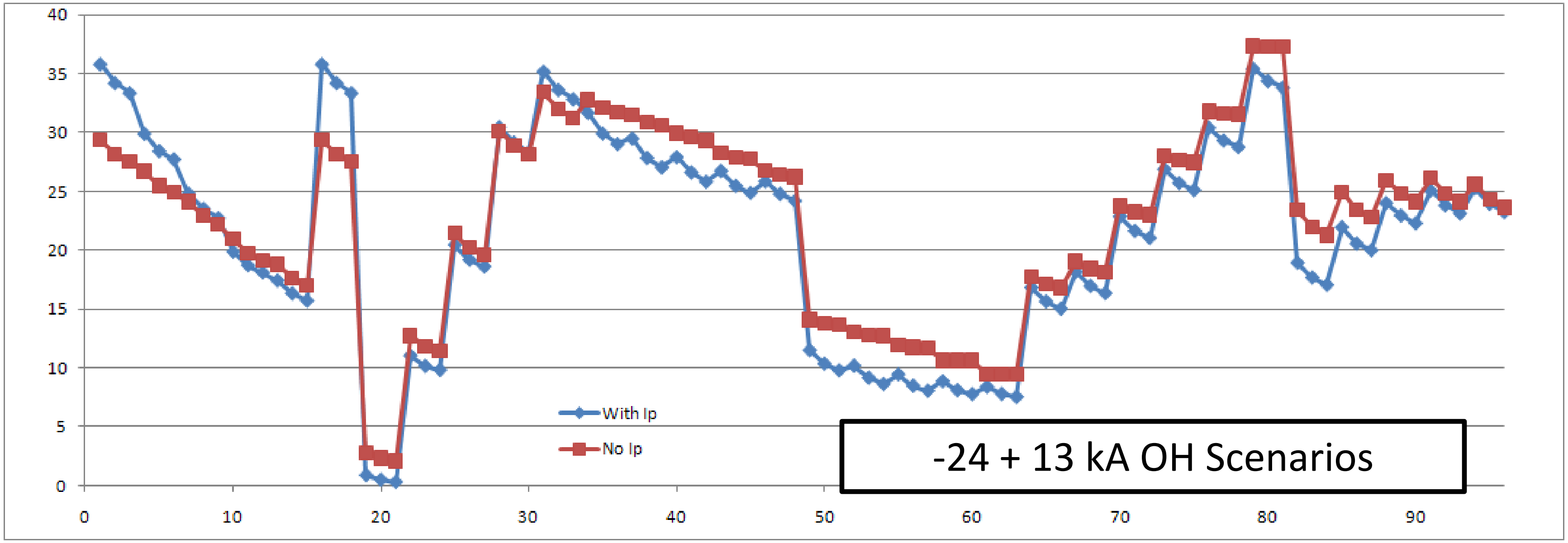
With Ip
No Ip
-24 + 24 kA OH Scenarios



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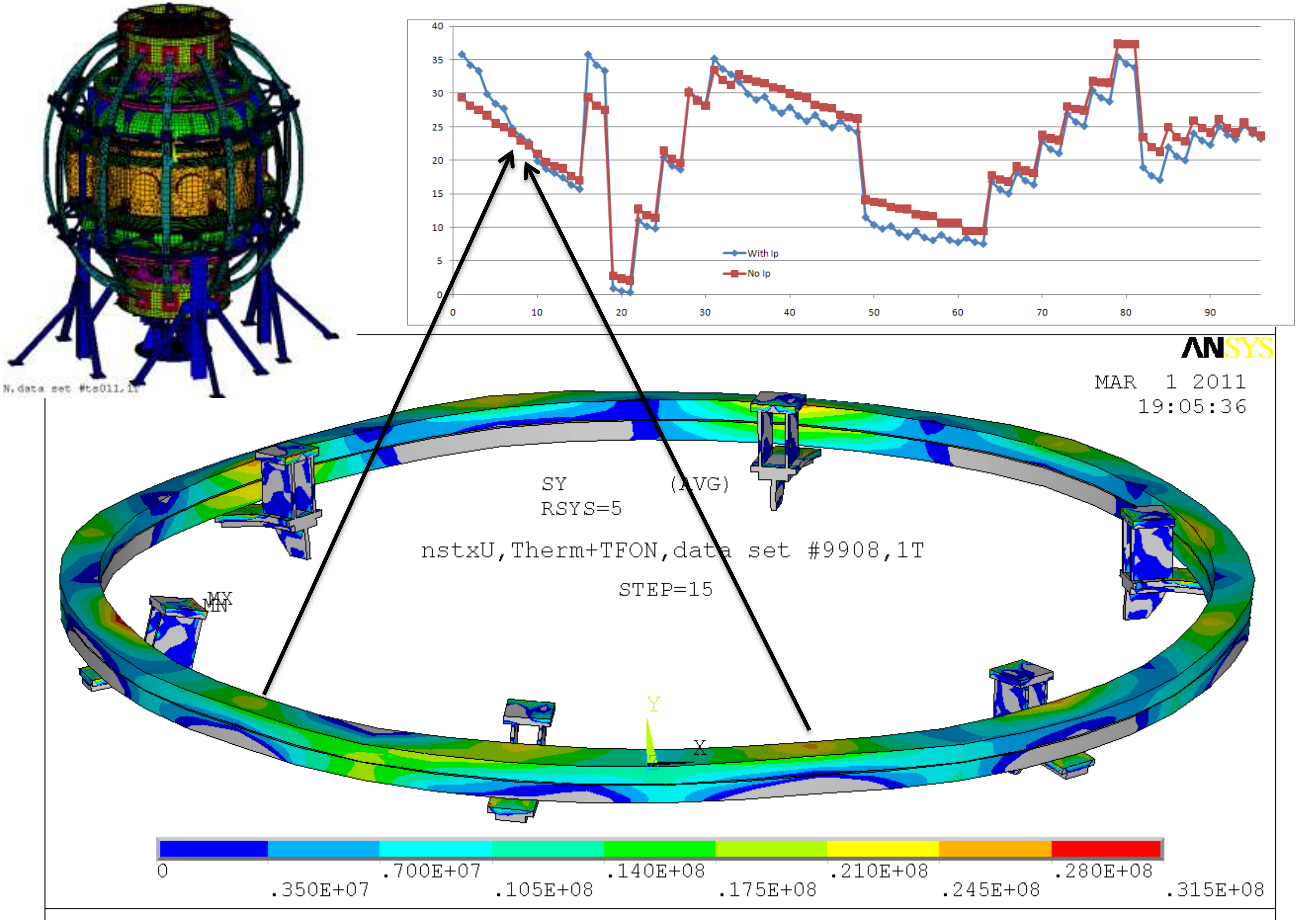
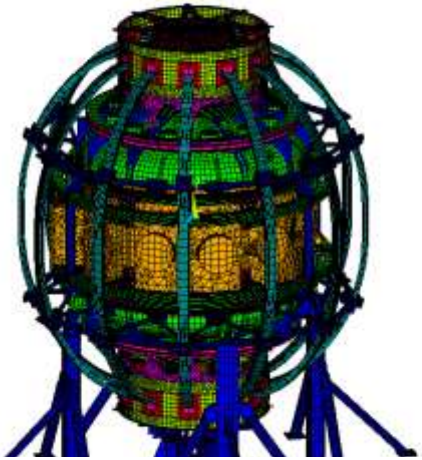
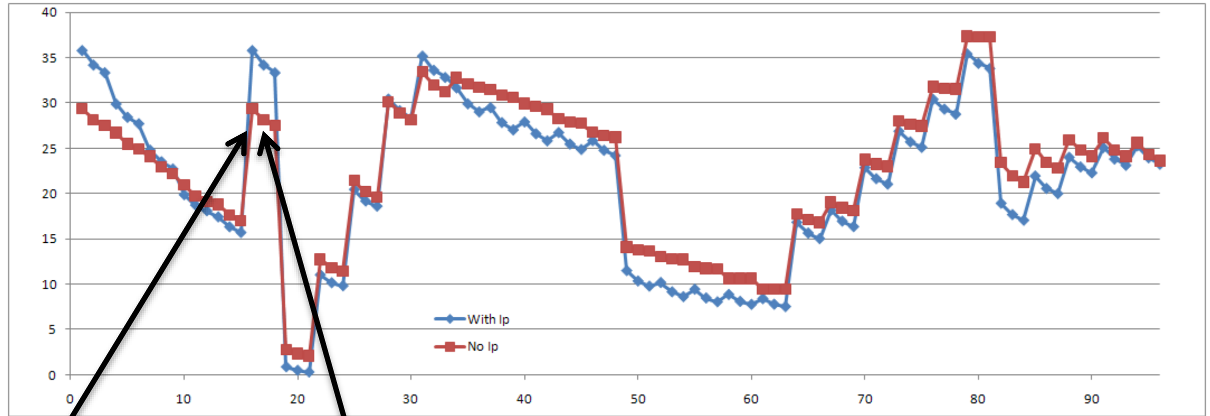
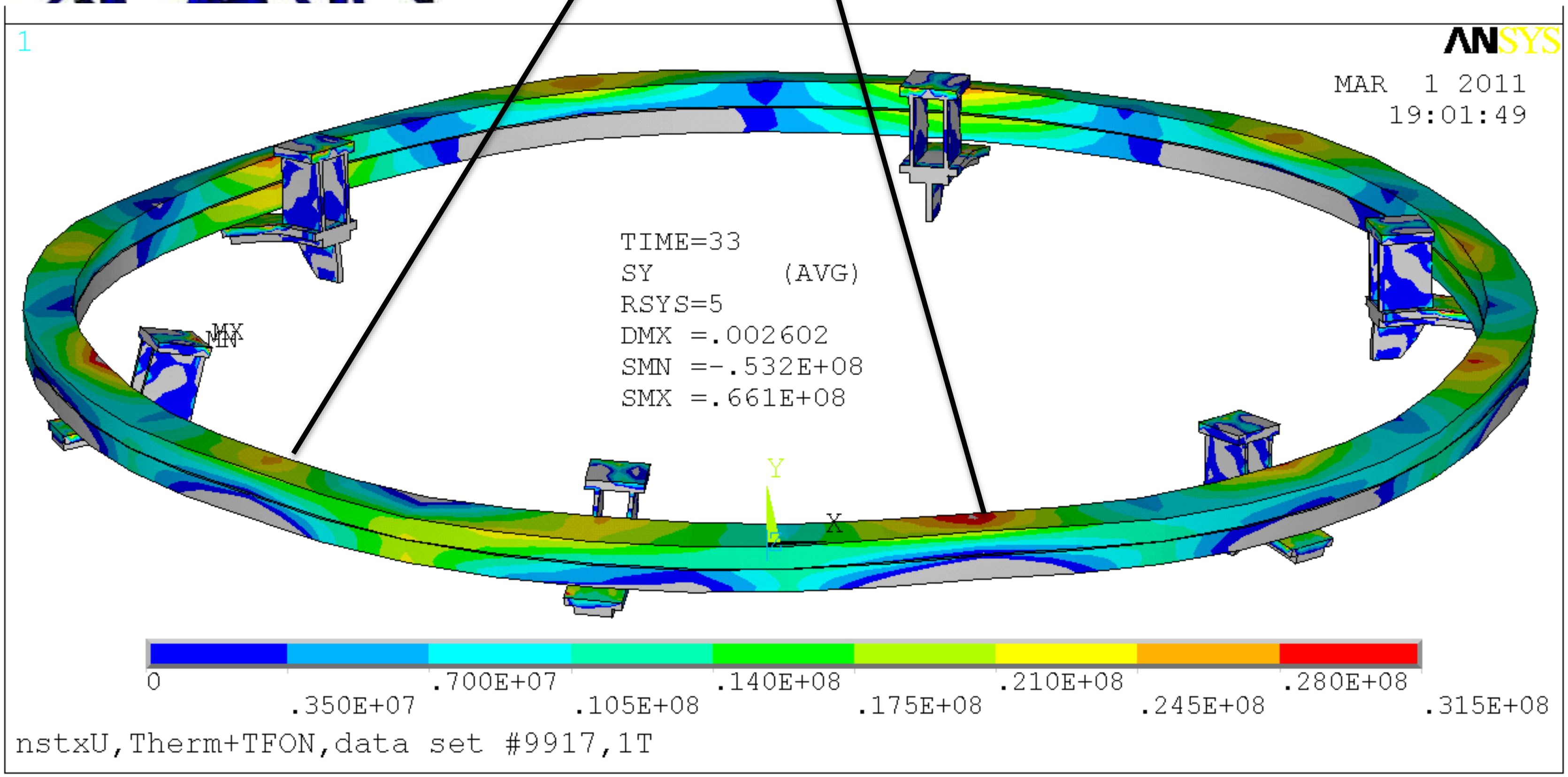
With Ip
No Ip
-24 + 13 kA OH Scenarios



Check Influence Coefficients Against Global Model

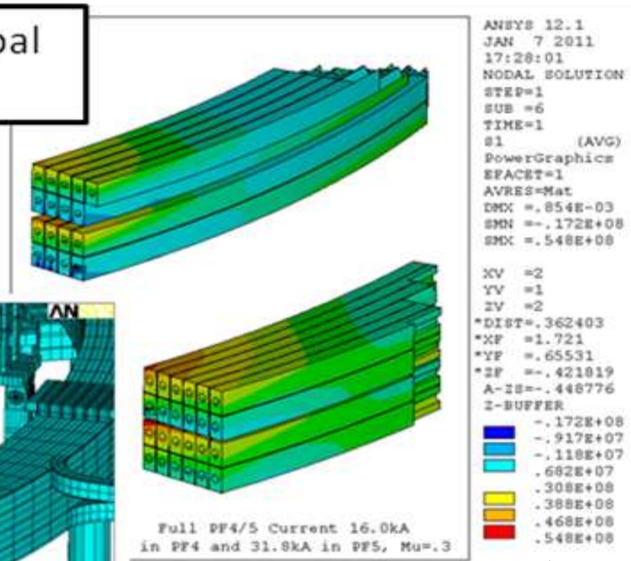


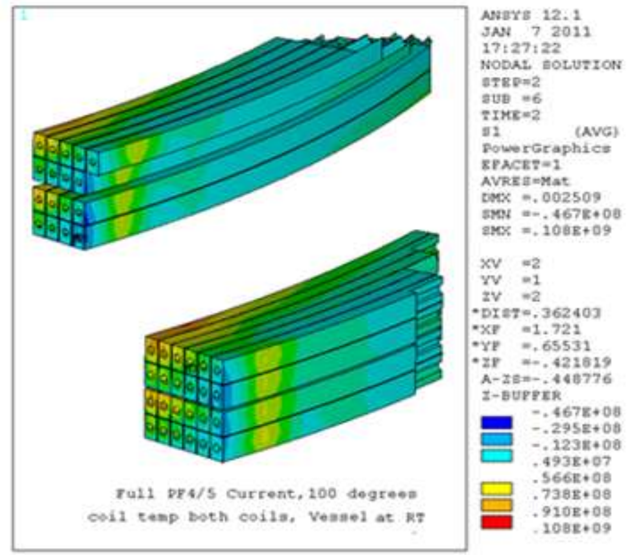


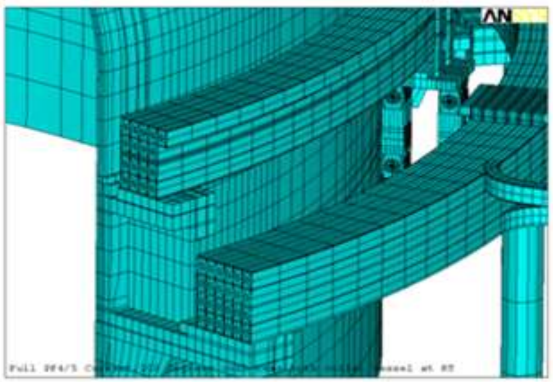


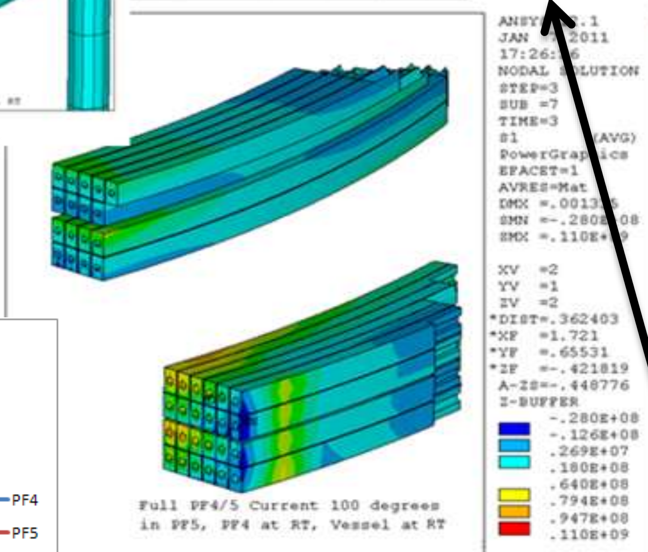
Check Influence Coefficients Against Global Model

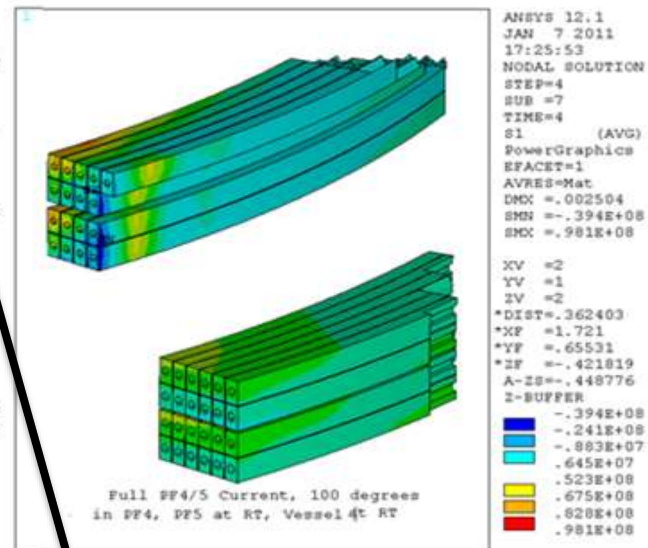
PF 4 and 5 Max Principal Stresses

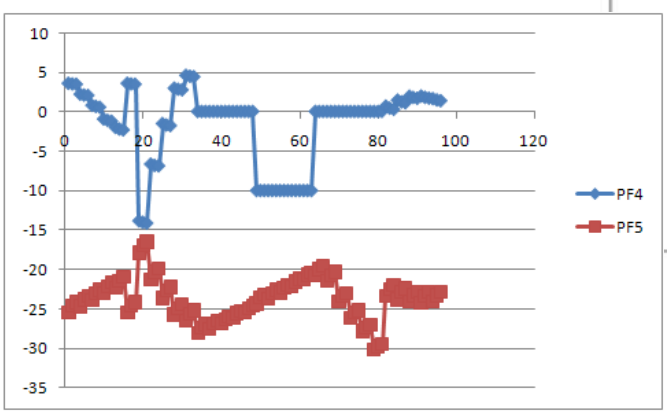












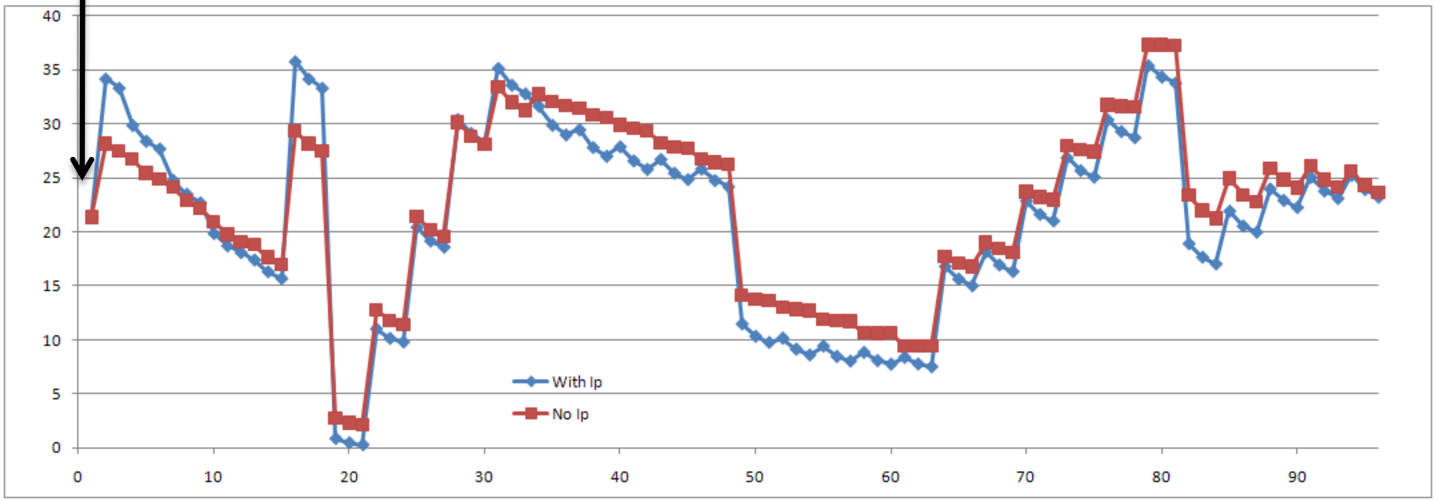
Full Current in PF4 and 5, 16 and 32 kA,

Produces 50 Mpa Conductor Stress With No Thermal

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
OH	PF1AU	PF1BU	PF1CU	PF2U	PF3U	PF4	PF5	PF1AL	PF1BL	PF1CL	PF2L	PF3L	PF4	PF5	ip
0	0	0	0	0	0	16	32	0	0	0	0	0	16	32	0
0	-6.07	9.4451	13.3051	2.9049	-8.822	3.482	-24.5839	-6.07	9.4451	13.3051	2.9049	-8.822	3.482	-24.5839	2
13.0237626	-5.8489759	10.1476777	14.3719632	5.46775943	-7.876963	3.44423109	-24.13404	-5.8489759	10.1476777	14.3719632	5.46775943	-7.876963	3.44423109	-24.13404	2
-24	-1.4573	6.2247	6.7393	-2.2799	-10.2215	2.1806	-24.6842	-1.4573	6.2247	6.7393	-2.2799	-10.2215	2.1806	-24.6842	2
0	-1.2113	7.8008	9.0773	2.1979	-8.4659	2.071	-23.82	-1.2113	7.8008	9.0773	2.1979	-8.4659	2.071	-23.82	2
13.0237626	-1.0236493	8.5927533	10.2738039	4.66796512	-7.478427	2.0253083	-23.38663	-1.0236493	8.5927533	10.2738039	4.66796512	-7.478427	2.0253083	-23.38663	2

Full Current in PF4 and 5, 16 and 32 kA,

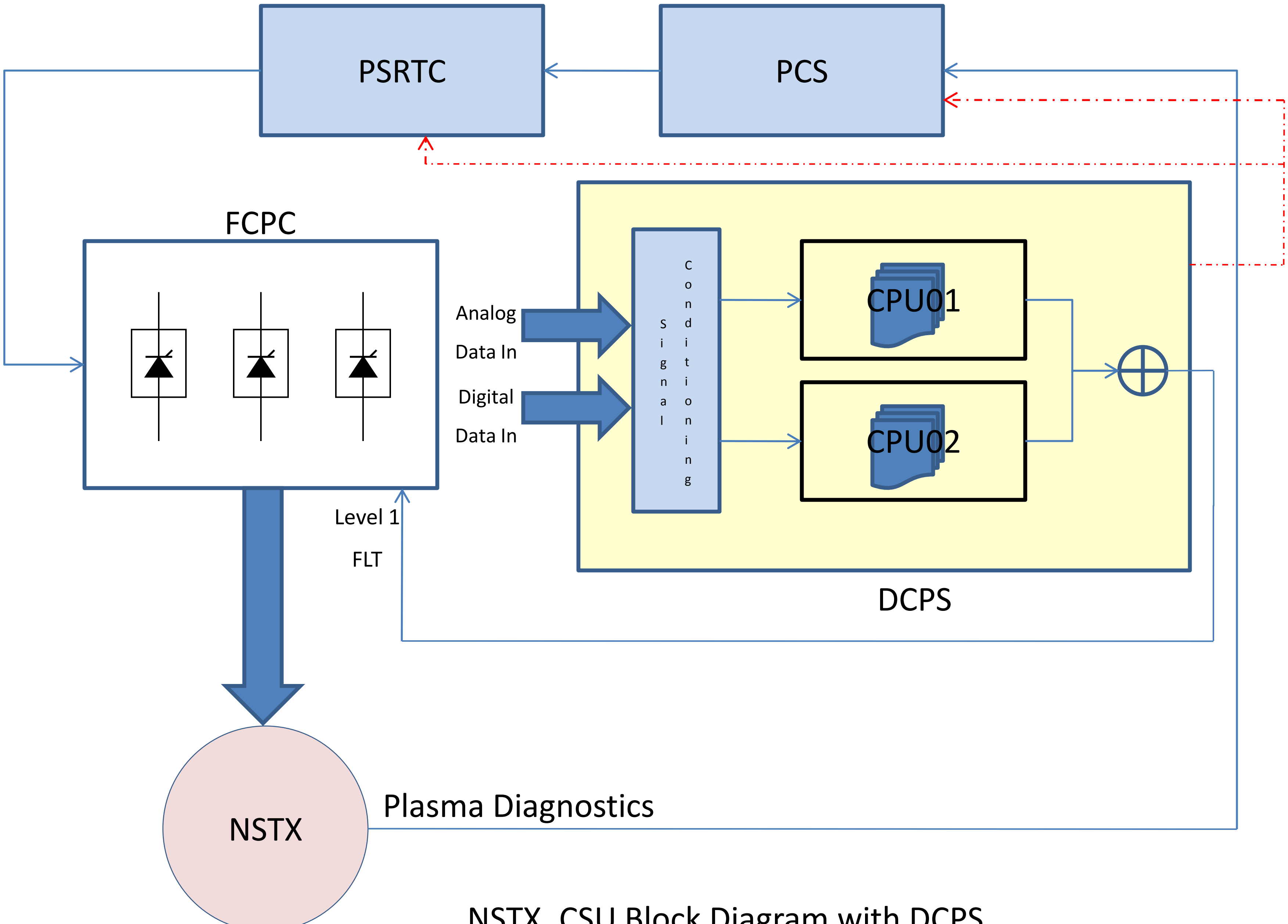
Produces 21 Mpa Smeared Stress from the influence coefficients



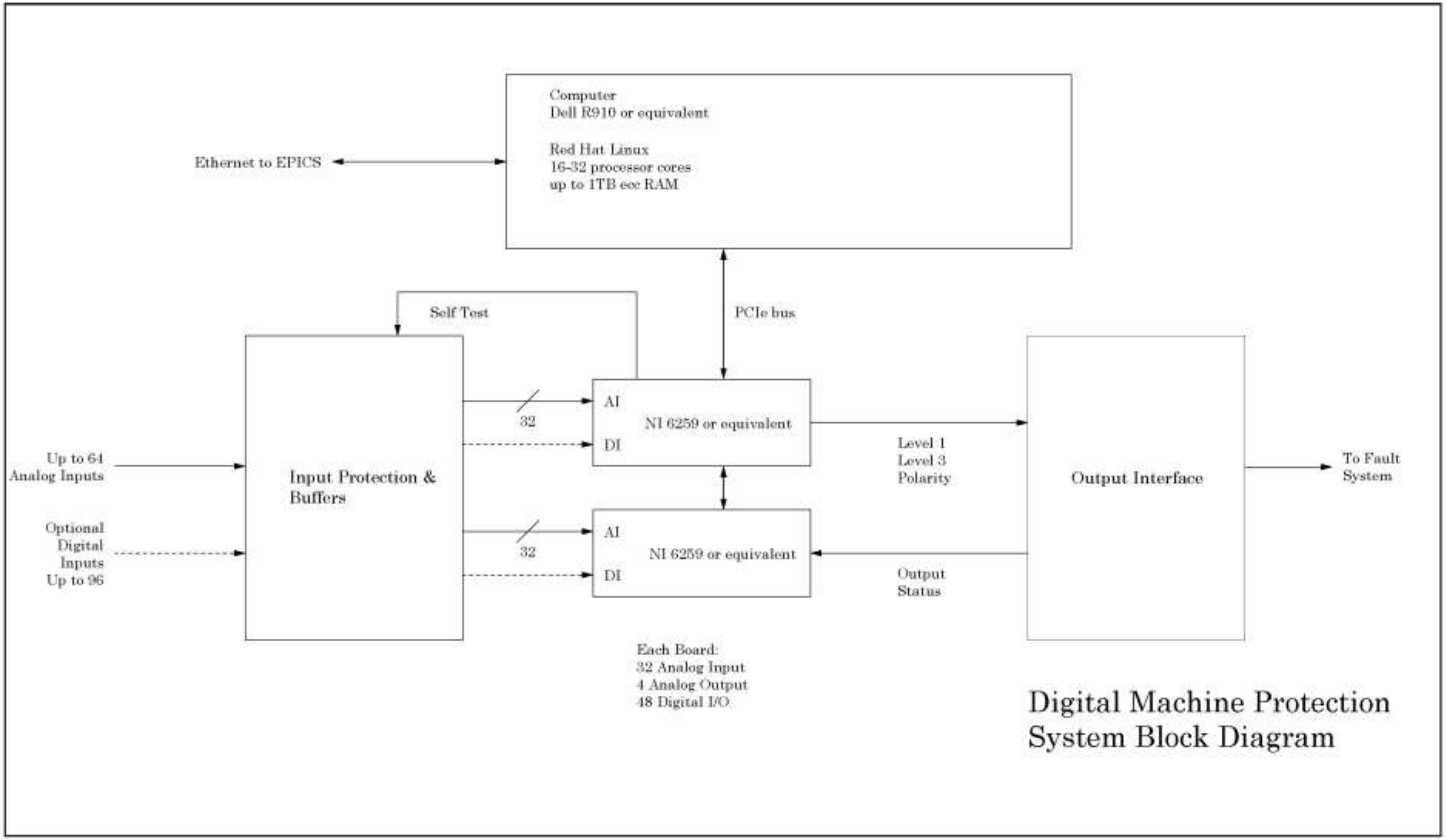
Multiply Influence Coefficient Results by 37/21 to get conductor stress?

DCPS protection list (mostly complete)

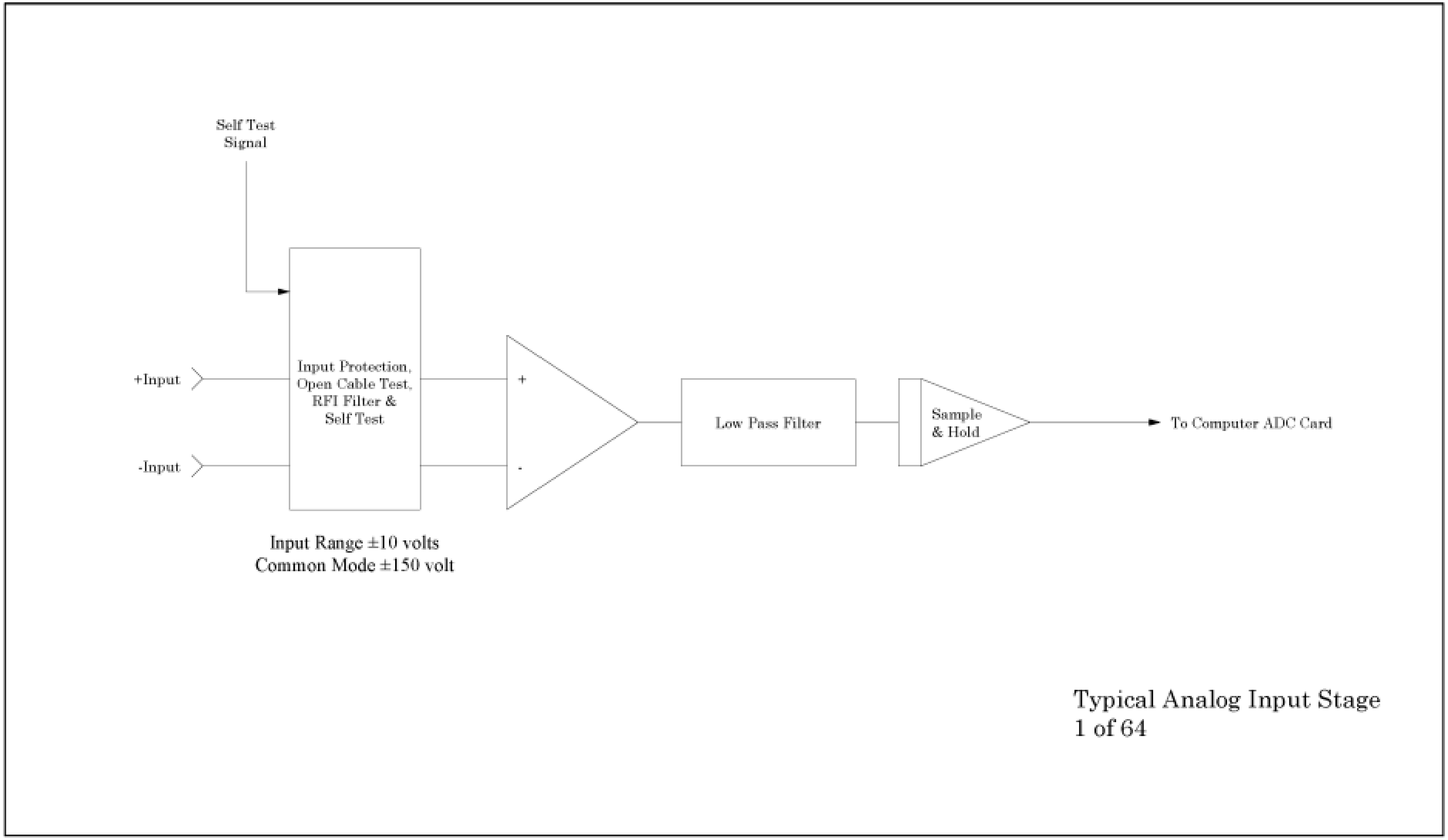
- PF coil supports
- Bus Bar stresses
- Outer leg insulation bond shear
- PF2 bracket and bolt stress
- PF3 bracket and weld stress
- Torques and stresses lid and spoke assembly (upper & lower)
- Vacuum vessel leg torque
- TF outer leg torque
- Forces on PF coils (single and combo)
- PF Coil moments (torque)
- Dome and PF rib stresses
- Coil thermal stresses
- Leg and brace Hilti's™ (loads and moments)
- Knuckle clevis loads
- Ring loads and moments
- Lid torque
- TF teeth torque
- TF joint bolts stresses
- Umbrella structure reinforcement (stress)
- OOP TF torque
- TF joint (forces, torques)
- TF coil torsional shear stress
- OH fatigue (long term)
- Shear forces between TF turns, insulation, and insulating crown
- Coil heating (i^2t)



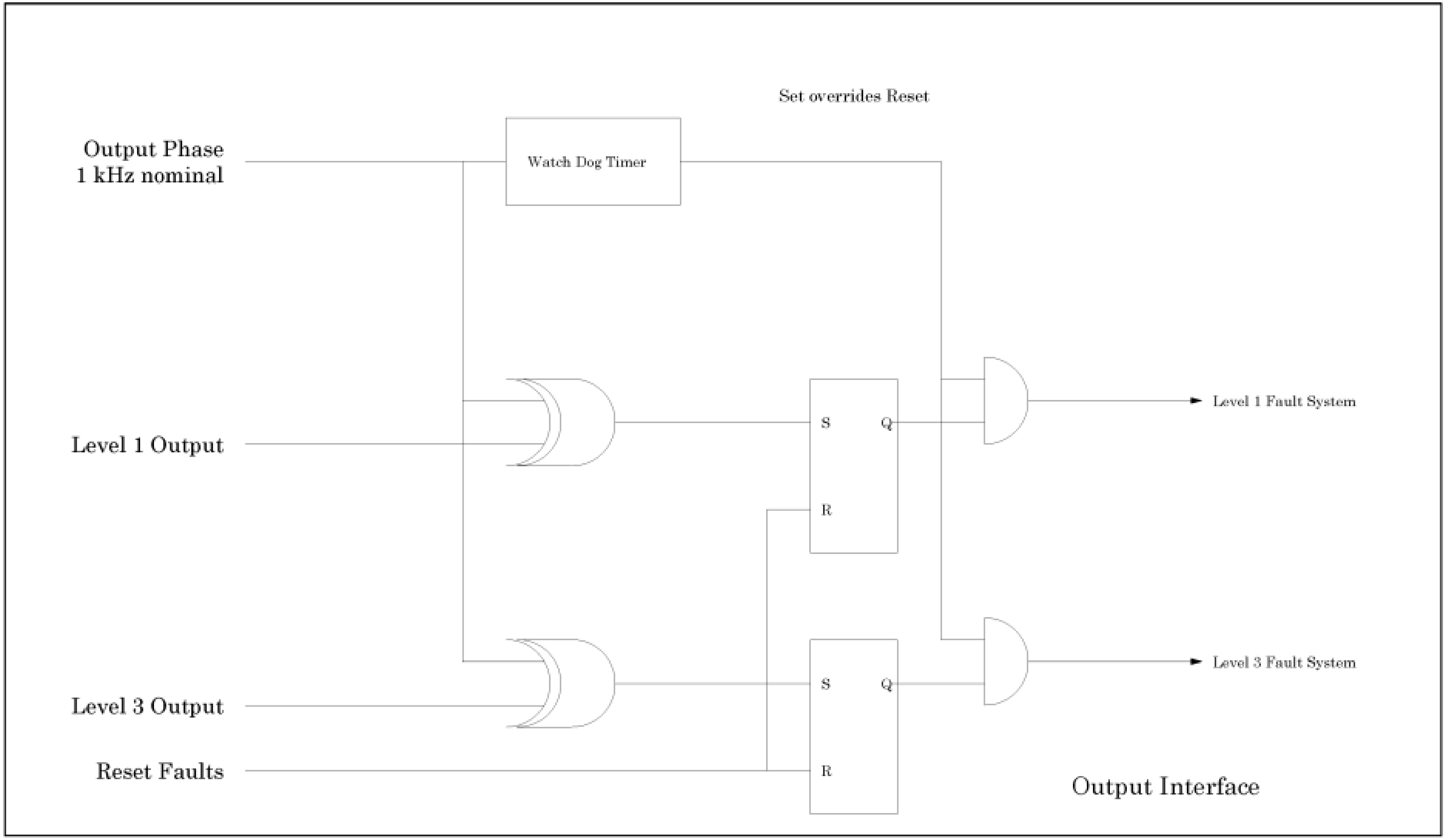
NSTX_CSU Block Diagram with DCPS



DCPS Hardware (1 of 2)



Analog Input Channel (typical)


Set overrides Reset
Output Phase
1 kHz nominal
Watch Dog Timer
Level 1 Output
S
Q
R
Level 1 Fault System
Level 3 Output
S
Q
R
Level 3 Fault System
Reset Faults
Output Interface

Next steps

1. Get paperwork in order (work planning form, NEPA, reviewed/signed requirements document)

2. A reasonable subset of algorithms to R. Woolley to program into DCPS simulation code

3. Commence preliminary hardware design (Lawson/Mozulay/Que(?))

4. Communicate with others in the community (ideas, see what they're doing)

5. Prepare for PDR to occur prior to project FDR (6/11)