NSTX-U

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NSTXU Digital Coil Protection System Overview

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Princeton Plasma Physics Laboratory

NSTX Upgrade Project

Readiness for Operations Review

December 9-11, 2014

Coll of Wm & Mary
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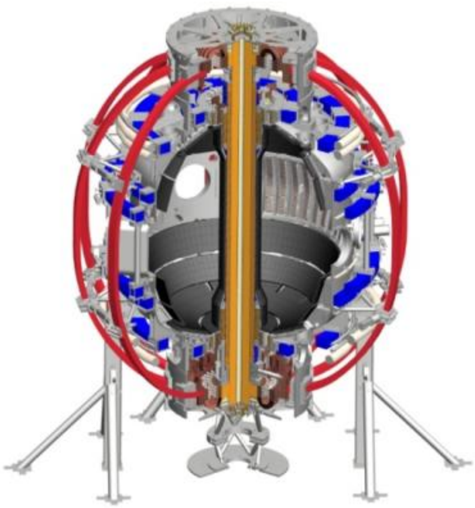

Culham Sci Ctr
York U
Chubu U
Fukui U
Hiroshima U
Hyogo U
Kyoto U
Kyushu U
Kyushu Tokai U
NIFS
Niigata U
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JAEA
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Ioffe Inst
TRINITI
Chonbuk Natl U
NFRI
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POSTECH
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ASIPP
CIEMAT
FOM Inst DIFFER
ENEA, Frascati
CEA, Cadarache
IPP, Jülich
IPP, Garching
ASCR, Czech Rep

Why DCPS?

- Plasma control system can direct power supplies to overload the machine structures
- TFTR era Power Supply capability can deliver coil overcurrent and overheating
- Structural solutions prohibitive and prohibitively expensive
- Previous analog overcurrent and I^2t too limited and would require upgrade anyway

So…

- Digital Coil Protection System envisioned:
  - Replaces previous analog and software coded limits
  - Updates to NSTXU coil set
  - Improves software architecture and code maintainability
  - Allows for more sophisticated and multiple types and instances of algorithms
  - Allows for auctioneering of currents for input checking
  - Upgrade Water System PLC (WSPLC)
  - Upgraded Pulse Duration & Period chassis (PDP)
  - Performs algorithms SoP to EoP (during the time window of a plasma shot)
  - Performs zero current checking EoP to SoP (non- shot interim)
  - Provides self-checking WatchDog Timer (WDT) to issue a fault if down
  - Provides Autotester for code and system testing
  - Provides Hardware User Interface for status, investigation, and reset of faults

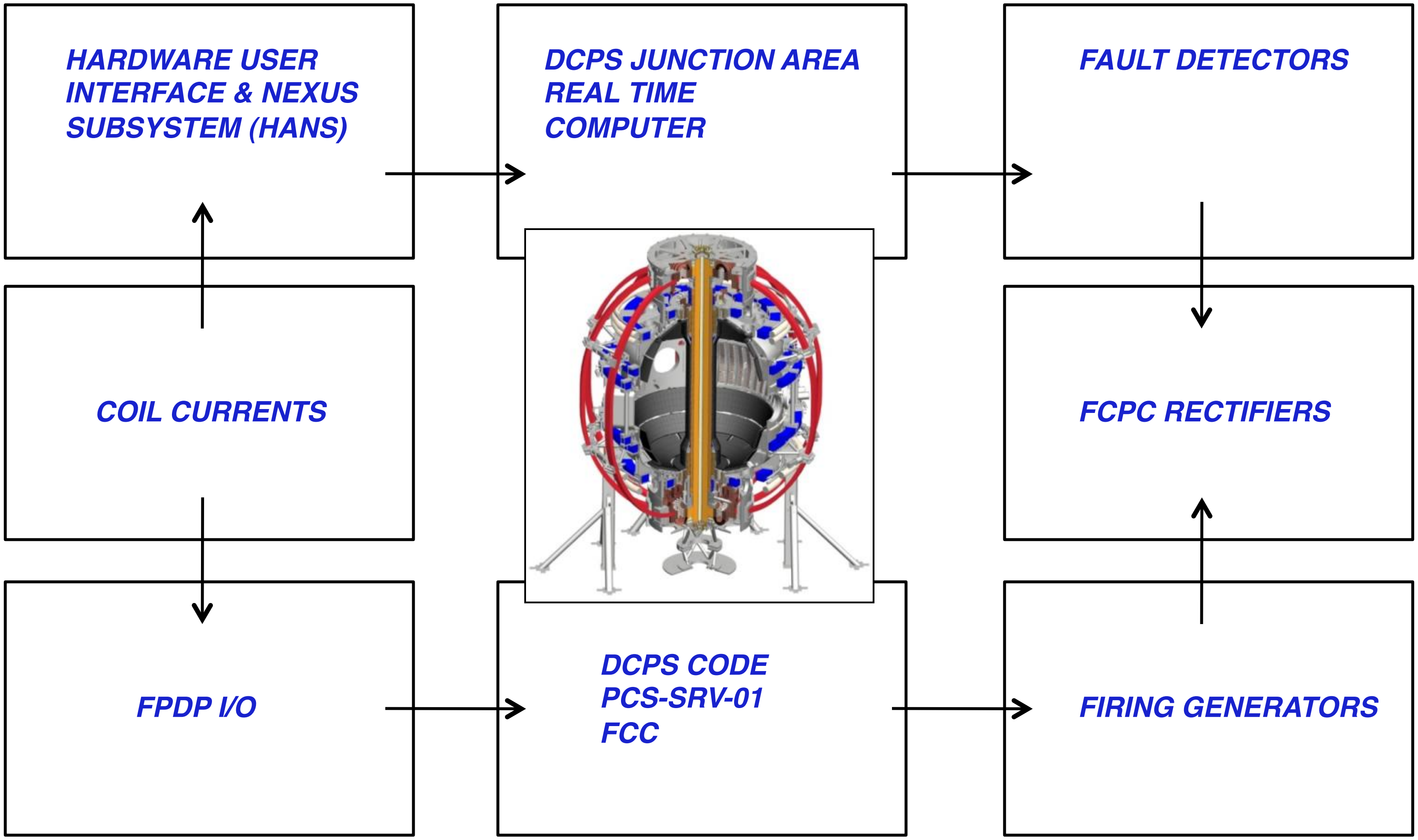
Requirements for DCPS

- NSTX_CSU_RQMT-CPS-159
- Protect the coils and machine from electromagnetic loads
- Read currents
- Perform Calculations called Algorithms
- Issue Level 1 Faults if fault conditions met – shut down the power
- Watchdog Timer Fault if code hangs or computer quits
- Algorithms performed every 200 microseconds between SoP and EoP
- Detect non-zero currents EoP to SoP
- Do not fail – high reliability

So…

- Two parallel and redundant trails to travel but same core code
- DCPS real time computer in D site FCPC Junction Area
- DCPS code residing on PCS-SRV-1 in NSTX Control Room FCC
- Same response effect
  - DCPS-FCC fault turns off power supplies through real time control
  - DCPS-JA fault trips off power supplies through L1 fault system
  - WDT trips L1 fault

Two Independent Redundant Paths for DCPS Protection



HARDWARE USER INTERFACE & NEXUS SUBSYSTEM (HANS)

DCPS JUNCTION AREA REAL TIME COMPUTER

FAULT DETECTORS

COIL CURRENTS

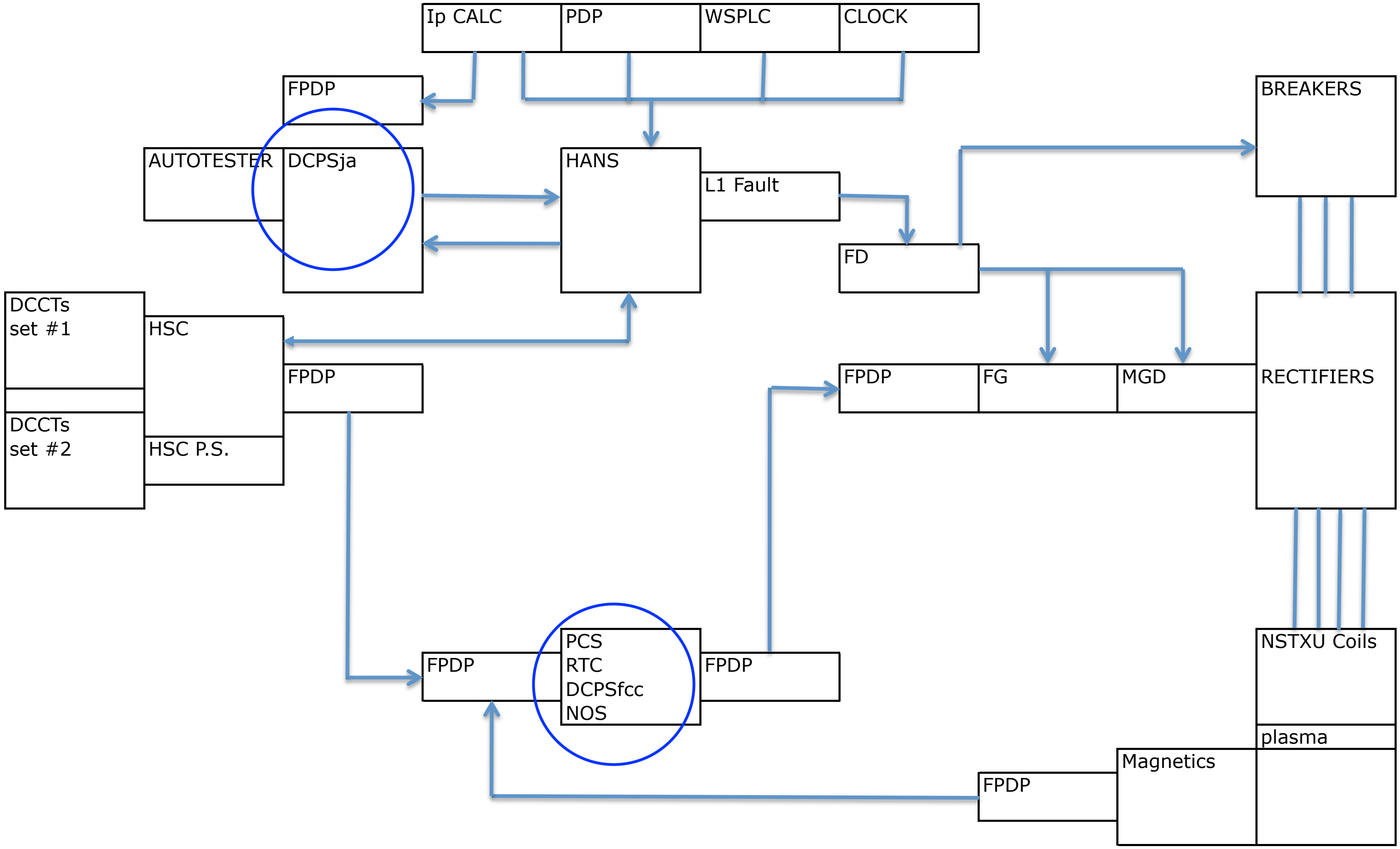
FCPC RECTIFIERS

FPDP I/O

DCPS CODE
PCS-SRV-01
FCC

FIRING GENERATORS

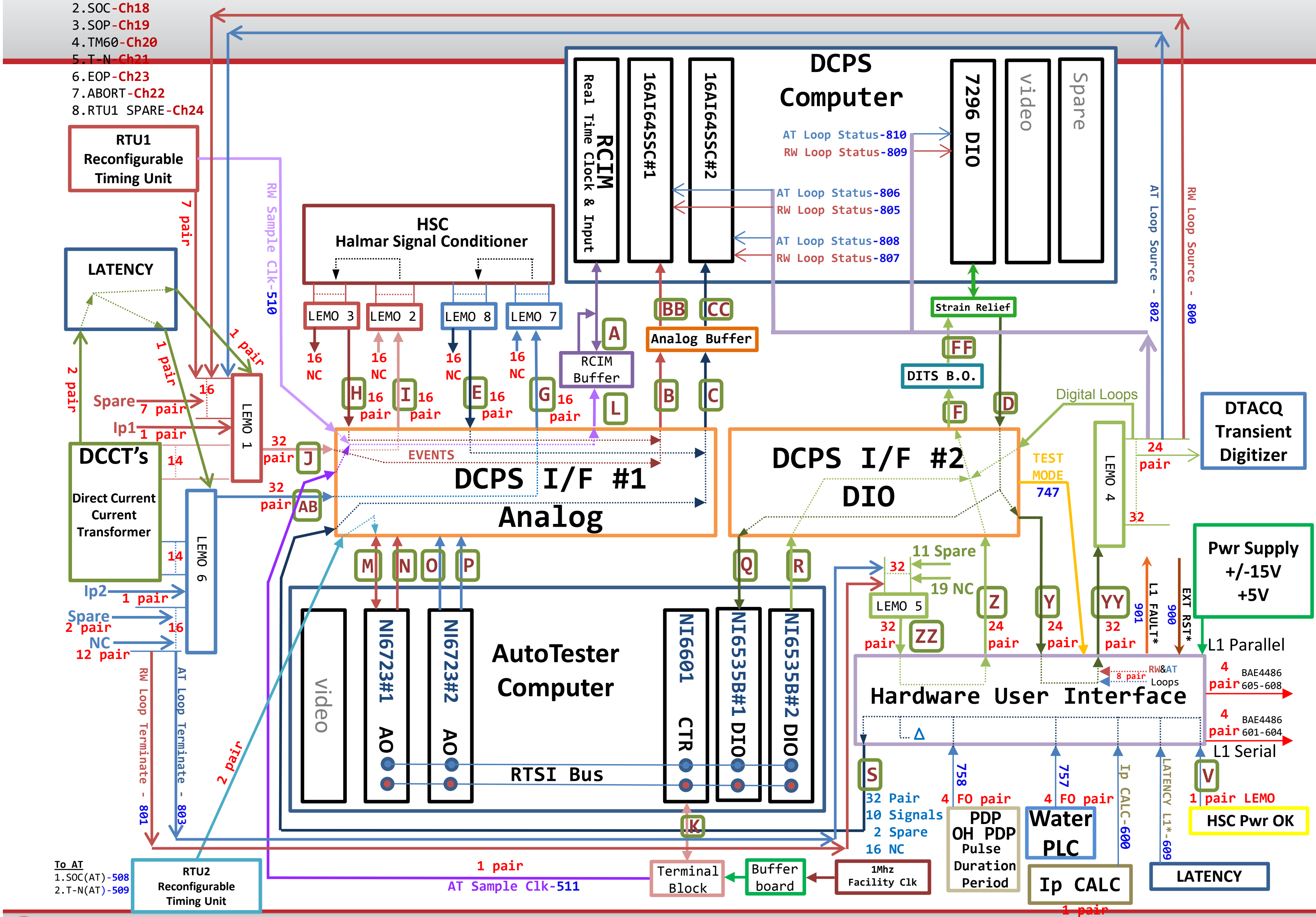
Simplified Block Diagram for DCPS – 2 places



Interconnection Diagram

24Oct2014/ps-jd-hs

To DCPS
1.SAMPLE CLOCK
2.SOC-Ch18
3.SOP-Ch19
4.TM60-Ch20
5.T-N-Ch21
6.EOP-Ch23
7.ABORT-Ch22
8.RTU1 SPARE-Ch24



To AT
1.SOC(AT)-508
2.T-N(AT)-509

Reviews for DCPS

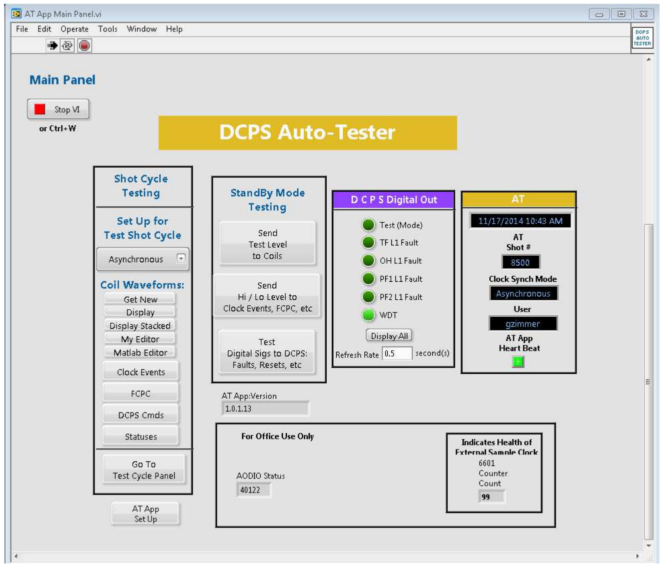
- NSTXU PDR, FDR, Office of Science Reviews
- Software CDR, PDR, FDR
- Hardware User Interface PDR, FDR
- Autotester Review
- Autotester Interface Chassis Review
- Real time Clock and Input Module (RCIM) Review
- Reconfigurable Timing Unit (RTU) Review
- Ip Calculator, PDP, WSPLC Reviews
- DCPS Code Review – 5 days, 3^+ hours each day
- PSRTC Software Review with imbedded DCPS integration
- Chits included in Project Chit Log per ENG-033 Design Verification procedure

DCPS Computer System Design

- Concurrent computers with Opteron processors
- Concurrent RedHawk Linux OS based on Red Hat Linux 6
- C++11 programming language
- Object Oriented design following UML standards
- Commonly available I/O cards
  - Redundant coil currents (16 x2 each) and Ip x2
  - Clock 5 kHz and clock events (SoP, EoP)
  - Analog and digital status signals
  - Output four L1 fault signals and Watchdog timer
- 200 microsecond cycle time on input data – hard requirement
- Trade off massive memory use for deterministic cycle
- Memory log of data without risking cycle time

DCPS Autotester

Screenshots from the DCPS Auto-Tester, Nov 2014 GNZ



AT: 11/17/2014 10:43 AM; AT Shot # 8500; Clock Synch Mode: Asynchronous; User: gzimmer

Refresh Rate 0.5 second(s)

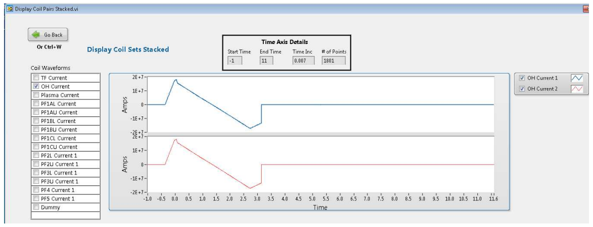
AT App:Version 1.0.1.13

AODIO Status 40122

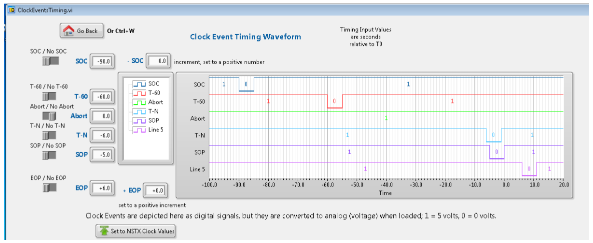
6601 Counter Count 99

The Autotester Main Panel

AT is a useful utility on a stand alone computer with analog output cards programmed in LabView and used in FCC and Junction Area locations.



Before the test shot cycle, verify the Coil Waveform you set up.

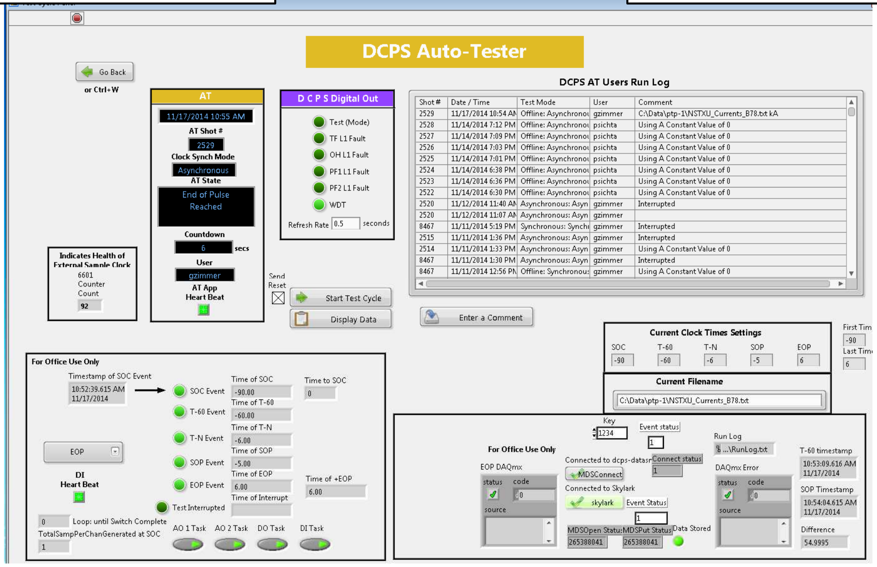


Clock Events are depicted here as digital signals, but they are converted to analog (voltage) when loaded; 1 = 5 volts, 0 = 0 volts.

Choose the timing for the clock events.

There are other panels similar to the above for setting up FCPC events such as the PDP Window and L1 Fault commands to the DCPS RT system.

Allows setup, synchronous clock and asynchronous clock operation with AT panel.



AT: 11/17/2014 10:55 AM; AT Shot # 2529; Clock Synch Mode: Asynchronous; AT State: End of Pulse Reached; Countdown 6 secs; User: gzimmer

Refresh Rate 0.5 seconds

6601 Counter Count 92

DCPS AT Users Run Log

Shot #	Date / Time	Test Mode	User	Comment
2529	11/17/2014 10:54 AM	Offline: Asynchronou	gzimmer	C:\Data\ptp-1\NSTXU_Currents_B78.txt kA
2528	11/14/2014 7:12 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2527	11/14/2014 7:09 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2526	11/14/2014 7:03 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2525	11/14/2014 7:01 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2524	11/14/2014 6:38 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2523	11/14/2014 6:36 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2522	11/14/2014 6:30 PM	Offline: Asynchronou	psichta	Using A Constant Value of 0
2520	11/12/2014 11:40 AM	Asynchronous: Asyn	gzimmer	Interrupted
2520	11/12/2014 11:07 AM	Asynchronous: Asyn	gzimmer	
8467	11/11/2014 5:19 PM	Synchronous: Synchr	gzimmer	Interrupted
2515	11/11/2014 1:36 PM	Asynchronous: Asyn	gzimmer	Interrupted
2514	11/11/2014 1:33 PM	Asynchronous: Asyn	gzimmer	Using A Constant Value of 0
8467	11/11/2014 1:30 PM	Asynchronous: Asyn	gzimmer	Interrupted
8467	11/11/2014 12:56 PM	Offline: Synchronous	gzimmer	Using A Constant Value of 0

Current Clock Times Settings

SOC	T-60	T-N	SOP	EOP
-90	-60	-6	-5	6

First Time -90; Last Time 6

Current Filename: C:\Data\ptp-1\NSTXU_Currents_B78.txt

Timestamp of SOC Event 10:52:39.615 AM 11/17/2014

Time of SOC -90.00; Time of T-60 -60.00; Time of T-N -6.00; Time of SOP -5.00; Time of EOP 6.00; Time of Interrupt; Time to SOC 0; Time of +EOP 6.00

EOP

Loop: until Switch Complete 0

TotalSampPerChanGenerated at SOC 1

Key 1234; Event status 1; Run Log ...\RunLog.txt; T-60 timestamp 10:53:09.616 AM 11/17/2014; SOP Timestamp 10:54:04.615 AM 11/17/2014; Difference 54.9995

EOP DAQmx; Connected to dcps-datasrv; Connect status 1; MDSConnect; Connected to Skylark; skylark; Event Status 1; DAQmx Error; MDSOpen Status 265388041; MDSPut Status 265388041; Data Stored

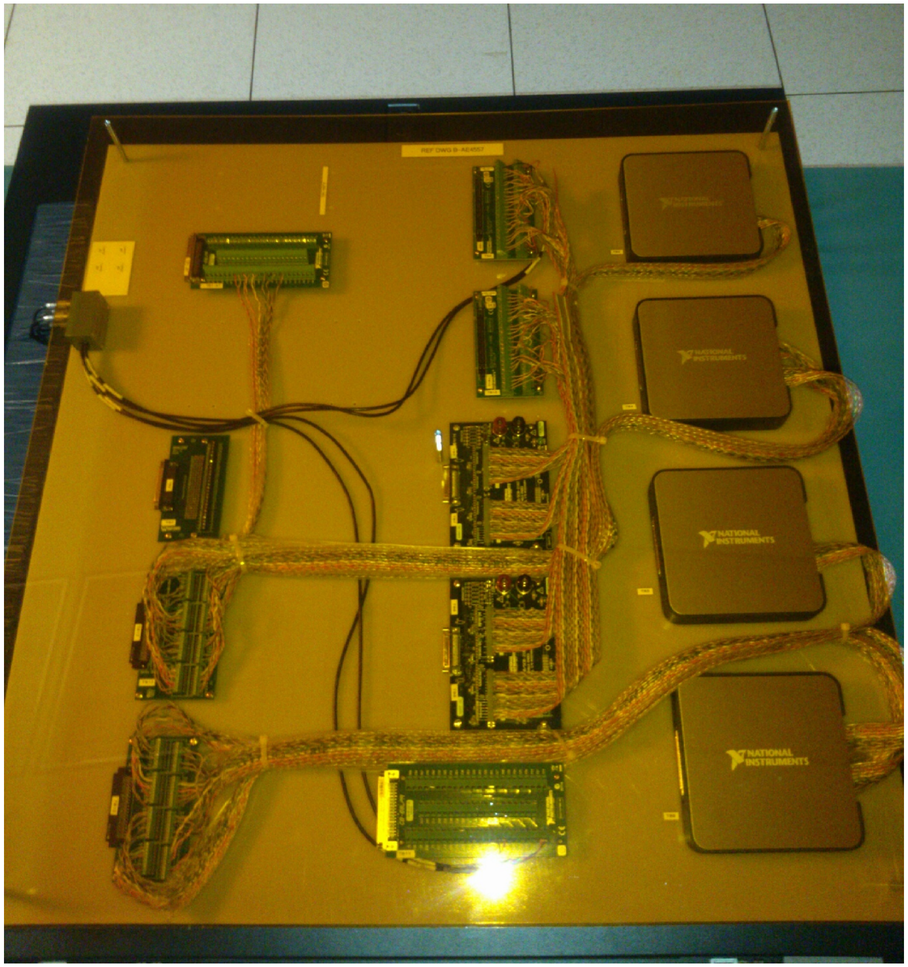
The Test Cycle Panel

AT completed

Allows status and output code testing, algorithm testing with shot files

Also now used for PSRTC testing

DCPS Autotester Interface Panel completed



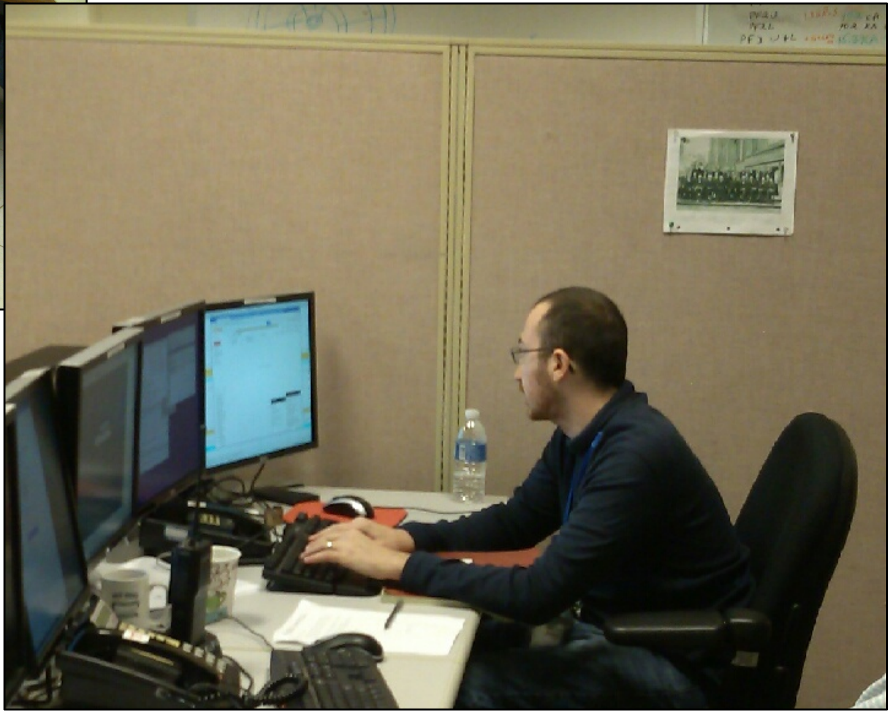
Allows local testing of DCPS code with Autotester

Testing of DCPS code with Autotester

Local code and AT testing began in FCC in Spring

Continued in Junction Area this summer

Then returned to FCC this Fall for remote testing



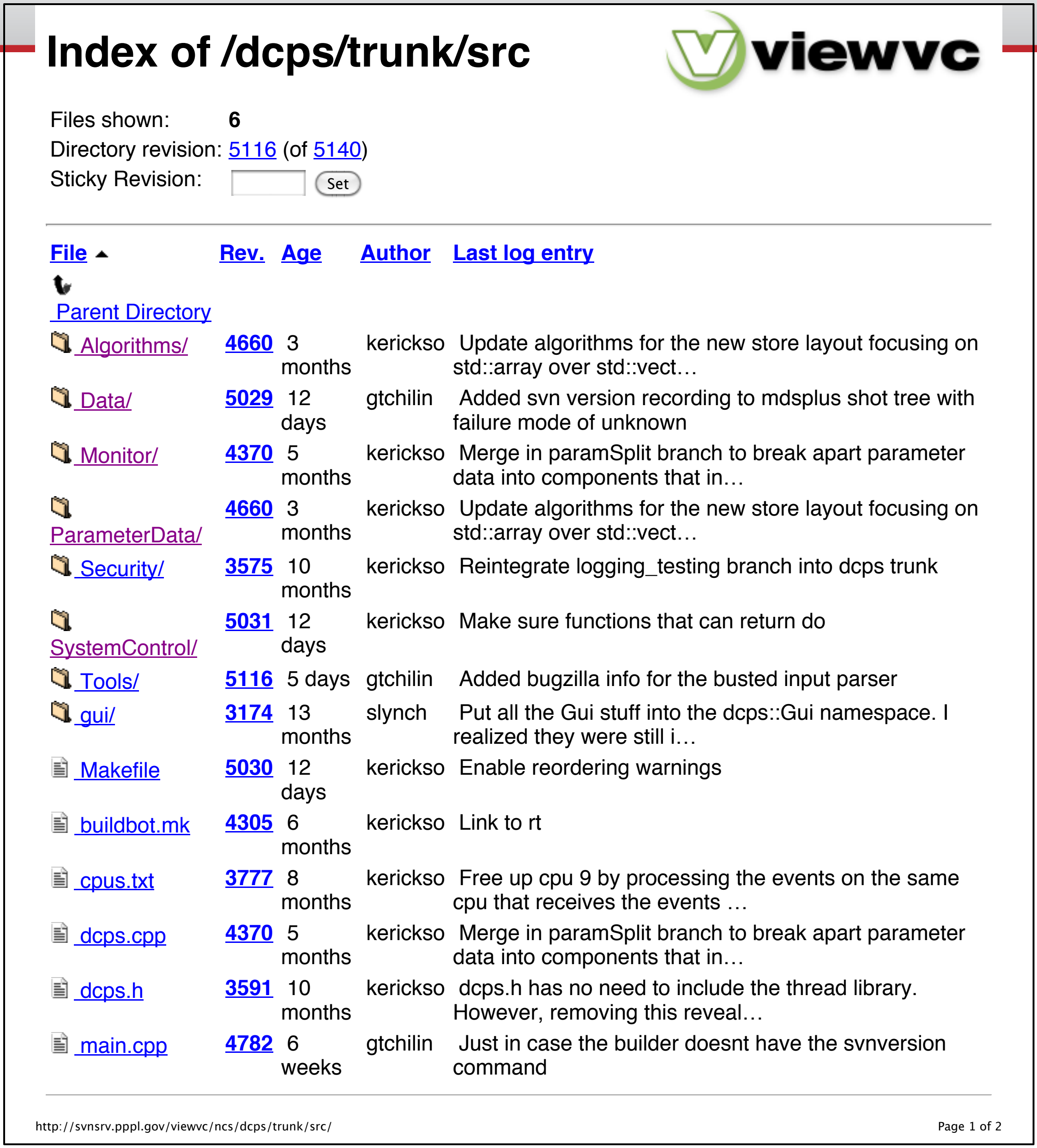
Well over 1500 test shots performed

Data archived and reviewed

Operator Log kept to track issues

Bugzilla used to collect punch list items

DCPS code configuration control using SVN SRV



Index of /dcps/trunk/src

Files shown: **6**

Directory revision: 5116 (of 5140)

Sticky Revision: Set

File ▲	Rev.	Age	Author	Last log entry
Parent Directory				
Algorithms/	4660	3 months	kerickso	Update algorithms for the new store layout focusing on std::array over std::vect…
Data/	5029	12 days	gtchilin	Added svn version recording to mdsplus shot tree with failure mode of unknown
Monitor/	4370	5 months	kerickso	Merge in paramSplit branch to break apart parameter data into components that in…
ParameterData/	4660	3 months	kerickso	Update algorithms for the new store layout focusing on std::array over std::vect…
Security/	3575	10 months	kerickso	Reintegrate logging_testing branch into dcps trunk
SystemControl/	5031	12 days	kerickso	Make sure functions that can return do
Tools/	5116	5 days	gtchilin	Added bugzilla info for the busted input parser
gui/	3174	13 months	slynch	Put all the Gui stuff into the dcps::Gui namespace. I realized they were still i…
Makefile	5030	12 days	kerickso	Enable reordering warnings
buildbot.mk	4305	6 months	kerickso	Link to rt
cpus.txt	3777	8 months	kerickso	Free up cpu 9 by processing the events on the same cpu that receives the events …
dcps.cpp	4370	5 months	kerickso	Merge in paramSplit branch to break apart parameter data into components that in…
dcps.h	3591	10 months	kerickso	dcps.h has no need to include the thread library. However, removing this reveal…
main.cpp	4782	6 weeks	gtchilin	Just in case the builder doesnt have the svnversion command

http://svnsrv.pppl.gov/viewvc/ncs/dcps/trunk/src/ Page 1 of 2

OP-DCPS-779 will require the appropriate code version and revision of DCPS software as part of setup, startup, and daily operations.

DCPS Hardware Design

- Fail safe
- Analog and digital signals
- Hardware User Interface And Nexus Subsystem (HANS)
  - Autotester mode and Real World mode – key cards to avoid error
  - 8 32 channel Lemo interface panels
  - Interfaces defined and maintained with DCPS Data Dictionary
  - Level 1 fault channels issued to FCPC L1 series and parallel circuits
  - Drawings complete
  - Installation complete
  - PTPs complete & punch list items in progress
- First use of DCPS-JA will be with Rectifier Dummy Load testing
- Interface buffer chassis with DCPS FCC in progress

On pace for CD-4….

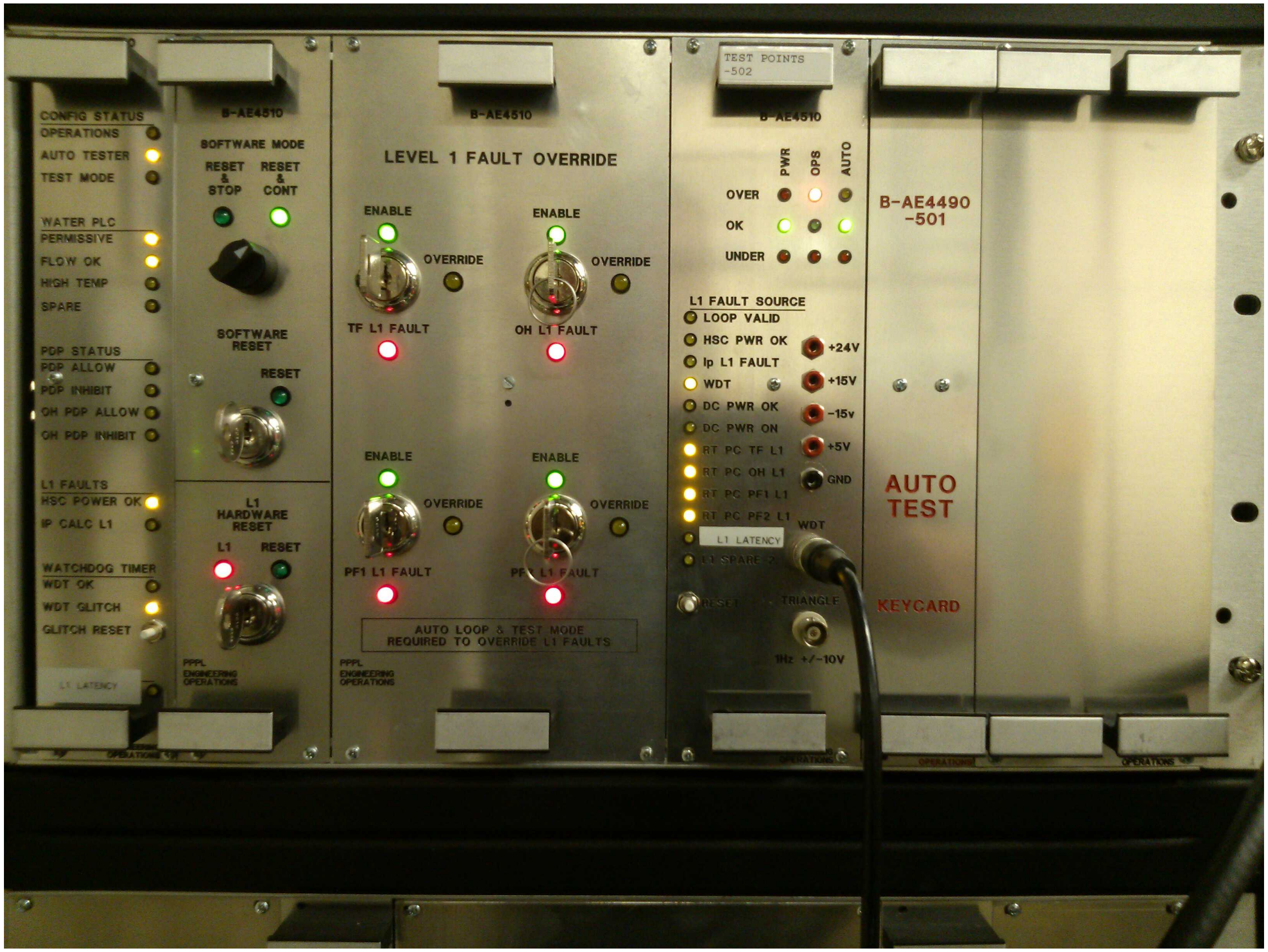
Board testing and Bench testing of DCPS Hardware completed

PTP-DCPS-002 and PTP-DCPS-003

Junction Area DCPS – Installation and testing completed

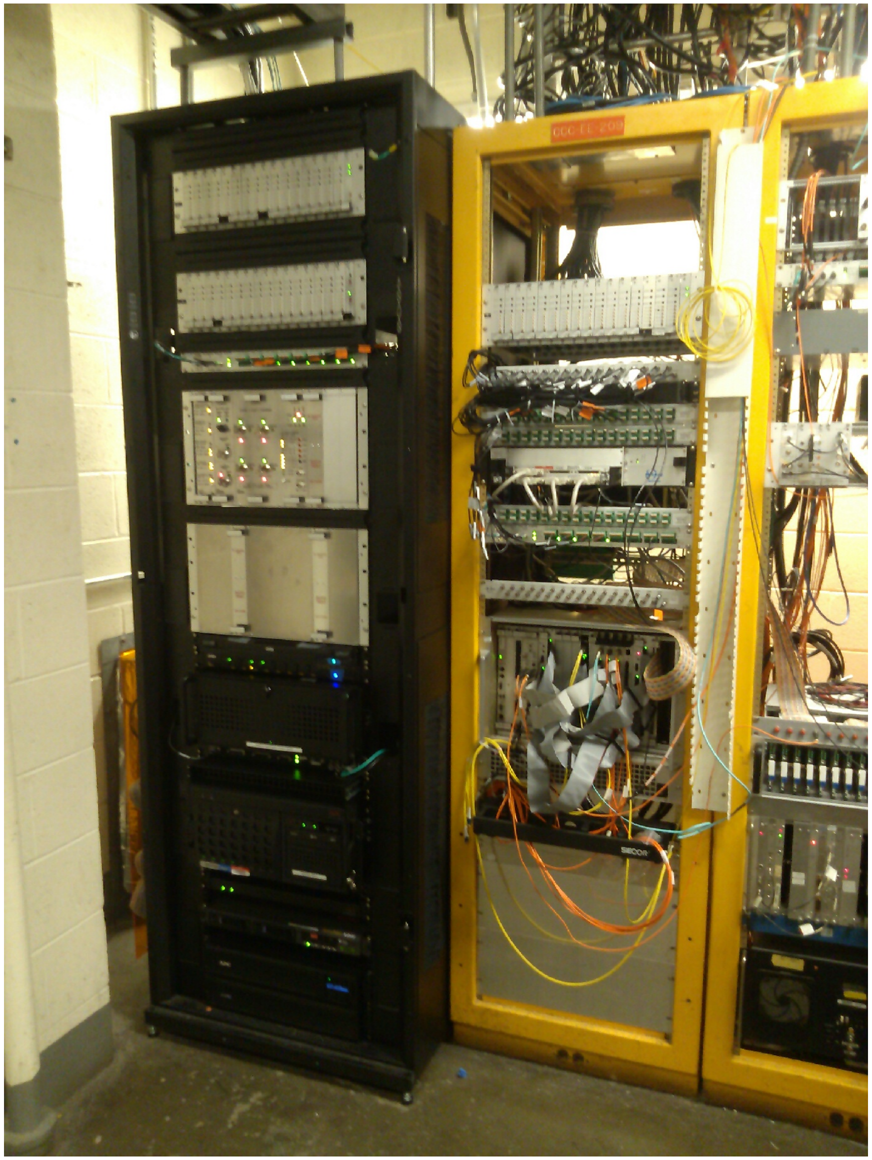
PTP-DCPS-003 and PTP-DCPS-004

Junction Area DCPS Hardware User Interface installed and tested



Keycards for Autotester mode and for Real World mode

DCPS Junction Area – ready to roll



HSCs

RTU

HUI

AIO/DIO

DCPS AT computer

DCPS-RT1 computer

Data Server

UPS

Interface testing in progress

First use of DCPS-JA will be in support of rectifier dummy load testing using OI and I^2t limits

Experience will be gained with operability and operations protocols prior to ISTP and CD-4

DCPS FCC residing on PCS-SRV-1

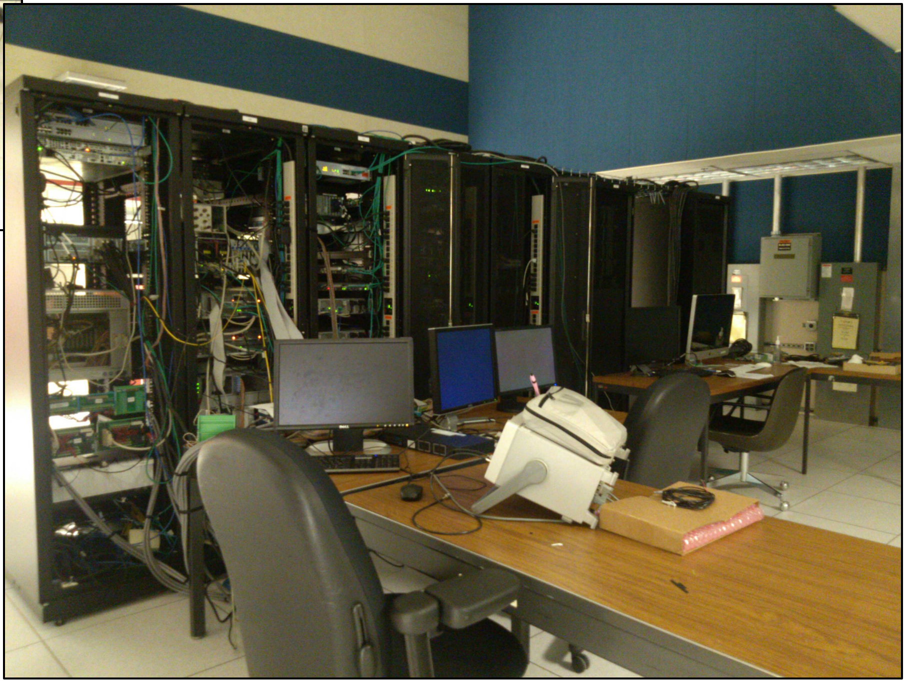
Redundant code using PCS inputs from FPDP data stream

Set slightly more restrictively than DCPS-JA to avoid L1

Same core code in both locations

DCPS core software testing completed

DCPS PCS Integration in progress



Testing found OS kernal problem

Concurrent computer out for recovery

DCPS fcc running on "Warthog" for testing

On track for CD-4…

Algorithms for DCPS code – so far…

- Basic Moment and Vertical and Radial Force per Coil
- Combined Vertical Force
- TF Shear Stress and Out of Plane Moment
- PF Bolt Stresses
- PF Hoop and Bending Stresses
- Local OH Stress
- Action - Coil Heating (I^2t) with appropriate margin for coil heating from fault
- Overcurrents (Derived Type I)
- Includes margin for effect of disruption and halo currents due to a VDE

New:

- $T_{OH} > T_{TF}$ with copper heating corrections due to Aquapour-CTD-425
  - (in development for CD4)

DCPS_PARAMETER TREE sets parameters…

- New tree created for each new set of parameter data
- Each post-shot archive contains the DCPS_param version used
- Data stored in a protected location
- Accessible by DCPS without a network switch
- Immutable within reasonable expectation
- Read-only to the outside world
- DCPS reads correct Param_tree for each shot every shot
- Administratively controlled by OP-DCPS-779 setup and startup procedure daily and with any requested or required change…

From K. Erickson Code Review

Provenance of Algorithm Limits for DCPS

- DCPS limits from Engineering Analysis or force/stress values from 96 scenarios
  - Documented in design and analysis calculations
- Machine qualified to operate all 96 GRD scenarios with nearly infinite variations within the protection envelope
- Much margin beyond the 96 scenarios in many cases
- Caveats:
  - PF3 bipolar dynamics and PF1A strikepoint control especially during VDE
  - Soft shutdown for off-normal plasma behavior being considered for PCS to avoid DCPS trips
- DCPS algorithms added to Designpoint Spreadsheet and checked/benchmarked against full spec shot and 96 scenarios
- DCPS C++ code mimiced in IDL with two years of NSTX operations data
  - Check loads, forces, stresses plotted against plasma current
- Evaluate and improve Test shots to avoid egregious operation of the machine

From Living with DCPS…, S. Gerhardt

Pre-Operational Test Procedures for DCPS

PTP-DCPS-001	Software Testing	Approved	Done
PTP-DCPS-002	Board Bench Testing	Approved	Done
PTP-DCPS-003	HUI Testing	Approved	Done
PTP-DCPS-004	Real World Testing	Approved	In progress
PTP-DCPS-005	Buffer Chassis Testing (New)	Working draft in progress	Dry runs in progress
OP-DCPS-779	Ops Setup/Startup/Reset	Working draft in progress	In development

Software testing for DCPS

- Software PTP tests:
  - Verification of input data stream
  - Verification of DCPS input and output data calibration factor
  - Timing and data acquisition system
  - Interpretation of shot sequence signals
  - DCPS code operation in asynchronous mode
  - DCPS code operation in synchronous mode (facility clock)
  - Algorithm verification using cleverly constructed input files
  - Level 1 Fault response verified
  - WDT response verified

So far well over 1500 test shots have been performed…

Hardware testing for DCPS

- Hardware PTP testing includes
  - Lemo connectors
  - Board bench testing
  - Chassis bench testing
  - In- situ Rack tests of HANS using Autotester mode
  - Rack and Integrated system tests using Real World mode using Autotester
  - Interface testing (L1, Ip Calc, PDP, WS PLC…)
- Many of these test steps repeatedly test chassis busses, boards, cables, interfaces etc…

DCPS SDD, FMEA, and Reliability Assessment

- SAD updated to include DCPS
- FMEA updated to include DCPS for single point failures
- DCPS System Design Description and Reliability Assessment document drafted for failure rate analysis per NSTX_CSU_RQMT-CPS-159
- Failure of DCPS defined as a case where a L1 fault is warranted but neither DCPSs issue a fault
- Two independent, parallel, redundant fault systems with reliability that exceeds 10^{-4}/ year and far exceeds 3.33 x 10^{-8} failures/shot requirements

&

- Human performance factors mitigated with administrative control per OP-DCPS-779 and PTP testing after any changes before returning to operations
- Human intervention by COE with EPICS annunciation and other tools

DCPS Overview Conclusion

- DCPS core software completed – new algorithms in development for Ops
- DCPS hardware completed – punch list items in progress
- DCPS reviews completed – chits dispositioned and most closed
- DPCS PTP testing completed – more planned for Ops
- DCPS operations procedure in progress to support Ops setup/startup/reset/change control
- DCPS System Design Description and Reliability Assessment drafted to document that DCPS meets or exceeds requirements
- NSTX Upgrade Project DCPS job scope completed and cost account closed
- Multiple conference papers have been published
- DCPS System turned over to Operations to support upcoming Power Systems Dummy Load testing, ISTP-001, CD-4, and Physics Operations