Calculation No: NSTXU-CALC-52-01-00 **Revision No: 0**

Title- Calculation of Suppress/Bypass Shutdown Currents For Inner PF Coils

Purpose of Calculation: (Define why the calculation is being performed.)

To quantify the overshoot in coil current after a shutdown command.

Codes and versions: (List all codes, if any, used)

None

References (List any source of design information including computer program titles and revision levels.)

[1] System Requirements Document for Power Systems, NSTX-U-SRD-006-00
[2] System Design Description for Power Systems, NSTX-U-SDD-PWR-R0
[3] Design Point Spreadsheet Calculations for NSTX Center Stack Upgrade, NSTX-U-CALC-10-03-00

Assumptions (Identify all assumptions made as part of this calculation.)

See section 3 of the calculation report

Calculation (Calculation is either documented here or attached)

See attachment

Conclusion (Specify whether or not the purpose of the calculation was accomplished.)

The calculations presented herein provide conservative estimates of the peak Inner PF Coil currents in case of overcurrent trips as well as probability of occurrence. If additional inductance is added to the circuits to reduce ripple then the peak currents will be less than estimated herein.

Cognizant Individual (or designee) printed name, signature, and date

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I have reviewed this calculation and, to my professional satisfaction, it is properly performed and correct.

Checker's printed name, signature, and date

See signature of A. Gao on attached. No longer working at PPPL; not available to sign this form.

National Spherical Torus eXperiment - Upgrade

NSTX-U

Calculation of Suppress/Bypass Shutdown Currents For Inner PF Coils

NSTXU-CALC-52-01-00

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NSTX-U CALCULATION
Table of Contents

NSTX-U CALCULATION

Record of Changes

Rev.	Date	Description of Changes	Revised by
0	3/8/18	Initial Release	

1 Purpose of Calculation

Analysis of the Inner PF Coils (PF1A/B/C) requires consideration of the electromagnetic forces that can be generated during both normal and off-normal events. During off-normal events, whenever a fault condition in any PF coil system triggers a protection action, it will lead to shutdown of the Transrex AC/DC thyristor converter power supplies by suppressing the gates to the rectifier bridge thyristors and firing the bypass thyristors on all PF coil power supplies. For each power supply, depending on the phase angle of the incoming AC voltage, additional volt-seconds will be applied to the that coil-power supply circuit that will result in a brief rise ("blip") of current, beyond the protection setting, before the current begins to fall. This effect is especially pronounced for the Inner PF coils since their inductances are relatively low.

Several levels of current limiting and protection are in place to limit overcurrent conditions, each with a particular setting above the nominal rated circuit current, referred to as headroom. In the sequence of protection, moving through the chain of protective devices, the headroom in the protection level increases and the probability of reaching the protection level decreases.

The mechanical design assessment of the coils must consider the off-normal events and the frequency of their occurrence in order to apply appropriate multipliers (K factors) to the allowable stresses.

The purpose of this calculation is to quantify the overcurrent levels in PF1A/B/C and their frequency of occurrence.

2 References

[1] System Requirements Document for Power Systems, NSTX-U-SRD-006-00
[2] System Design Description for Power Systems, NSTX-U-SDD-PWR-R0
[3] Design Point Spreadsheet Calculations for NSTX Center Stack Upgrade, NSTX-U-CALC-10-03-00

3 Assumptions

3.1 Protection Levels and Probabilities

Various control and protection systems limit the loading of the coils:

1) Current limit (regulator) feature in PSRTC/PCS that takes over when plasma control algorithms demand for too much current

2) DCPS 1 that trips at X1% overcurrent or other protection algorithm overload

3) DCPS 2 that trips at X2% overcurrent or other protection algorithm overload

4) Transrex power supply section overcorrect that trips at X3% overcurrent

5) AC feeder breaker overcurrent that trips at X4% overcorrect

The current limit mentioned in 1) will limit the current magnitude to within values that are less than or equal to 10% over the 96 equilibria current maxima. The headroom (% of current allowed above nominal, defined as 10% over the 96 equilibria current maxima) are typically set as follows:

X1 = 2%

X2 = 5%

X3 = 10%

X4 = 20%

So, going from 1) to 5) above, there is some decreasing probability of occurrence and some increasing overcurrent trip level.

Based on engineering judgment the following assumptions are applied to the above cases:

1) Plasma control demand problem, once per operating day, current limited to 10% over equilibria levels

2) DCPS 1 failure, once per operating year, i.e. 10 x over lifetime of NSTX-U, 10 pulses out of 20000, $P = 5 \times 10^{-4}$, current limited to 10% + 2% over equilibria levels + blip current

3) DCPS 2 failure, once per 10 years, i.e. once over lifetime of NSTX-U, 1 pulses out of 20000. $P = 5 \times 10^{-5}$, current limited to 10% + 5% over equilibria levels + blip current

4) Limited to fault cases within FCPC that are unrelated to coil overcurrents

5) Limited to fault cases within FCPC that are unrelated to coil overcurrents

3.2 Circuit Behavior

3.2.1 Circuit configurations

Circuit configurations are given in Figure 1. The two types, unipolar PF1A, and bipolar (anti-parallel) PF1B and PF1B, exhibit different shutdown response and need to be treated separately in this analysis.

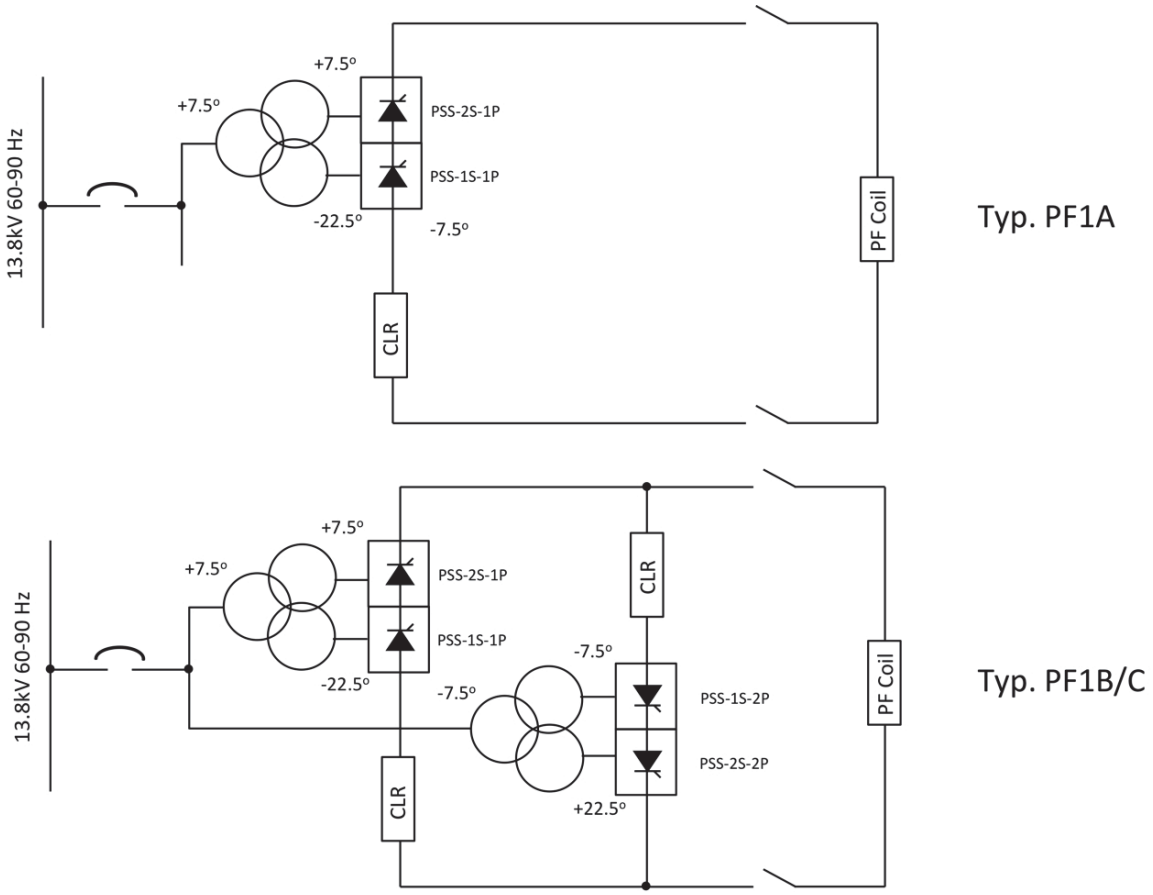


Figure 1 – Inner PF Coil Power Supply Configurations

It is noted that Current Limiting Reactors (CLRs) with impedance equal to the original TFTR design are assumed in all cases. Other considerations (e.g. harmonic ripple in load current) may require the additional inductance that would be added by new or supplemental inductors in the circuit. In any case the calculations herein are conservative because they do not account for any additional inductance. It is assumed that the power supply in the circuit in question is running flat out at thyristor phase control angle $\alpha = 0^{o}$, producing maximum output voltage, with the maximum number of power supply sections connected in circuit (2 PSS, 2kV open-circuit voltage), as the

current reaches the overcurrent protection level. Source frequency is assumed at 60Hz and source impedance is neglected. DC coil inductances are assumed. It is known that the mutually coupled passive structure tends to reduce the effective coil impedance but the effect is not predominant at 60Hz and compensated by neglecting the AC source impedance.

3.2.2 Initial conditions prior to suppress/bypass

Suppress/bypass event is assumed to occur at a multiple of 30^o into the sine wave as the coil current reaches the overcurrent trip level. This results in maximum volt-seconds being applied to the load circuit during the shutdown transient.

3.2.3 Coupling with other PF circuits

Although the protection interlocking is such that any trip in any subsystem (TF, OH, PF) will initiate a shutdown of all systems, for purposes of simplification, the calculation of blip current is based upon one coil circuit acting independently of all others. This is based upon the following reasoning:

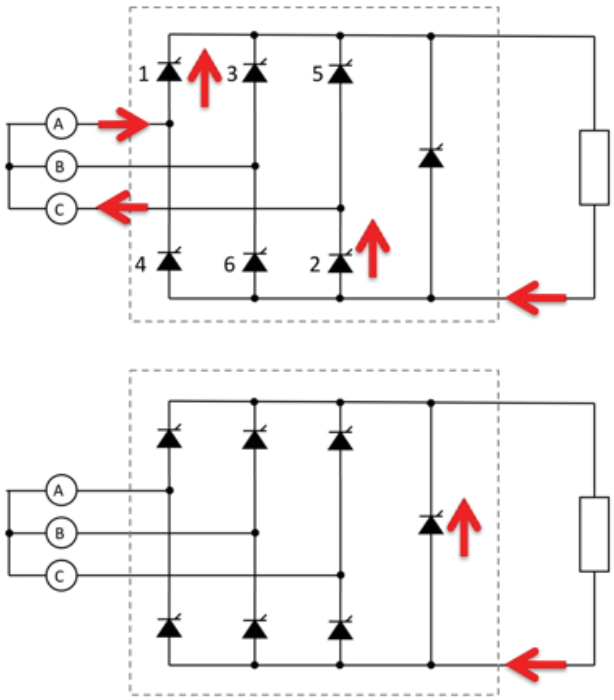
- It is improbably that multiple PF circuits would be encountering the same control failure as the circuit in question and would most likely experience a lesser blip owing to a different initial condition

- Initial conditions of coil currents in other PF circuits, in terms of magnitude and polarity, would lead to a mixture of addition to, and subtraction from, the blip in the circuit in question

4 Calculation

4.1 Power supply model

A simplified model of a Transrex AC/DC converter rectifier 6-pulse bridge is given in Figure 2. Prior to initiation of suppress/bypass shutdown, the load current flows through a pair of thyristors in the rectifier bridge and through two phases of the AC source. After the suppress/bypass event the gate pulses to the six bridge thyristors are suppressed and a gate pulse is issued to the bypass thyristors. Even though gate pulses to the bridge thyristors are suppressed, the last conducting pair continues to carry the current until it is commutated into the bypass. During this interval the AC source voltage waveform appears across the load. This condition is depicted in Figure 3 for the case of a 12-pulse converter formed by two 6-pulse PSS connected in series where the event is initiated at thyristor phase control angle $\alpha = 0^o$. This condition is consistent with a scenario where the current regulators have malfunctioned or the firing generator in the converter is stuck in a full-on state. It results in the maximum shutdown volt-seconds applied to the load and therefore the maximum current blip.



- Initial state
  - Bridge thyristors gated in order, bypass gate off
  - current flows into one phase of transformer and out the other
- Intermediate state
  - Bridge thyrisors gated off, bypass gated on
  - AC voltage applied across bypass
  - Bypass begins to conduct when forward biased, current begins to commutate from bridge thyristors to bypass
- Final state
  - bridge thyrisors gated off, bypass gated on
  - Load current flows through bypass

Figure 2 – Transrex AC/DC Converter Rectifier Suppress/Bypass Transient

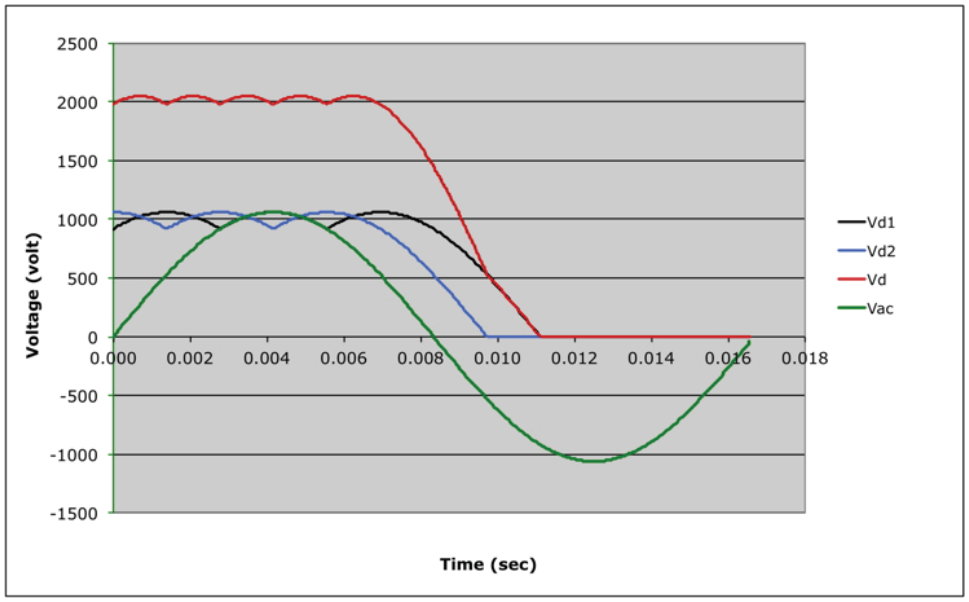


Figure 3 – Suppress/Bypass Transient from 12-pulse Converter Starting at α = 0°

In the case of the unipolar circuits of PF1A the V_d wave for shown in Figure 3 is applied directly to the load during the shutdown event. However, in the case of the bipolar circuits (PF1B and PF1C), since the suppress/bypass command is given to all of the PSS in the power supply, the bypass in the antiparallel branch that is not actively carrying the load current creates a circulating current loop between the two branches that results in ~ ½ of the voltage of the active branch appearing across the load, owing to the voltage divider effect of the two CLRs. This effect is depicted in Figure 4.

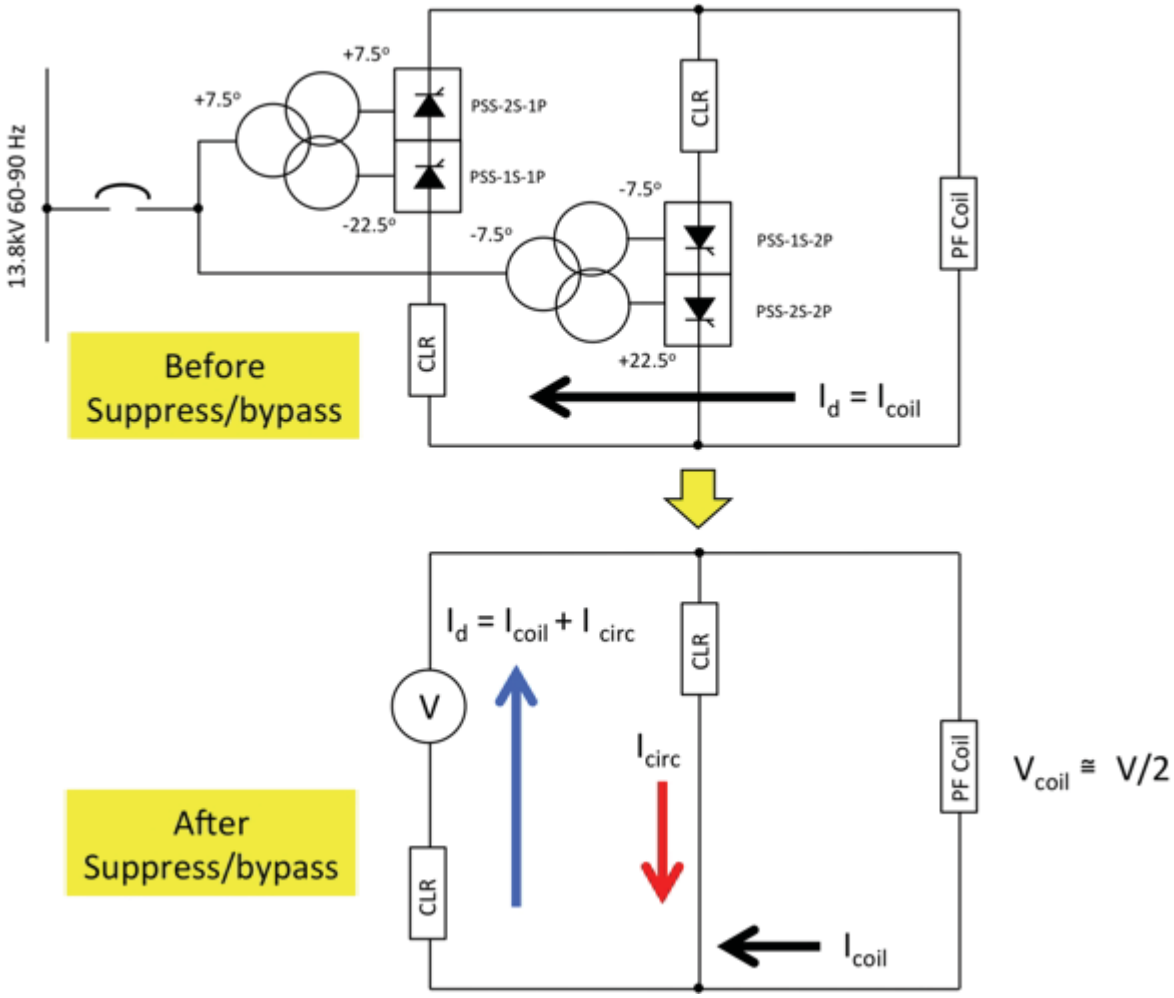


Figure 4 – Suppress/Bypass in Bipolar, Antiparallel Circuit

4.2 Approximate calculation of blip current

The incremental blip current driven in the coil will be determined by the volt-seconds applied to the circuit inductance after the transient is initiated. Referring to Figure 3, in

the worst case, the event will initiate when one of the AC voltage waveforms is at 60° and the other at 90°. In the case of the unipolar circuit the full voltage will be applied to the coil, in the case of bipolar, ½ of the voltage. The I x R drop will reduce the voltage applied to the coil inductance and can be approximated by an amount proportional to the coil current at the time of the trip, neglecting the change in current during the transient. So the blip current can be estimated as follows:

$$\Delta I \approx \frac{\int \left(\frac{V(t)}{n} - I_{trip} * R\right) dt}{L} = \frac{\frac{V_{ac}^{peak}}{n}\left[\int_{60}^{180} \sin(\omega t)\, dt + \int_{90}^{180} \sin(\omega t)\, dt\right] - I_{trip} * R * \Delta T}{L}$$

$$\Delta I \approx \frac{\frac{-V_{ac}^{peak}}{2\pi f n}[(\cos(180) - \cos(60) + \cos(180) - \cos(90)] - I_{trip} * R * \frac{(90 + \frac{60}{2})}{360f}}{L}$$

$$\Delta I \approx \frac{\frac{2.5V_{ac}^{peak}}{2\pi f n} - I_{trip} * R * \frac{120}{360f}}{L}$$

For the unipolar circuit transient the variable n=1, and for bipolar n=2.

4.3 Simulation of blip current

An XL simulation that produces the rectifier output voltage as a function of thyristor phase control angle α was adapted to include a simple Euler integration to solve for the coil current and circulating current (in case of bipolar). Typical worst-case results are given in Figures 5 – 8.

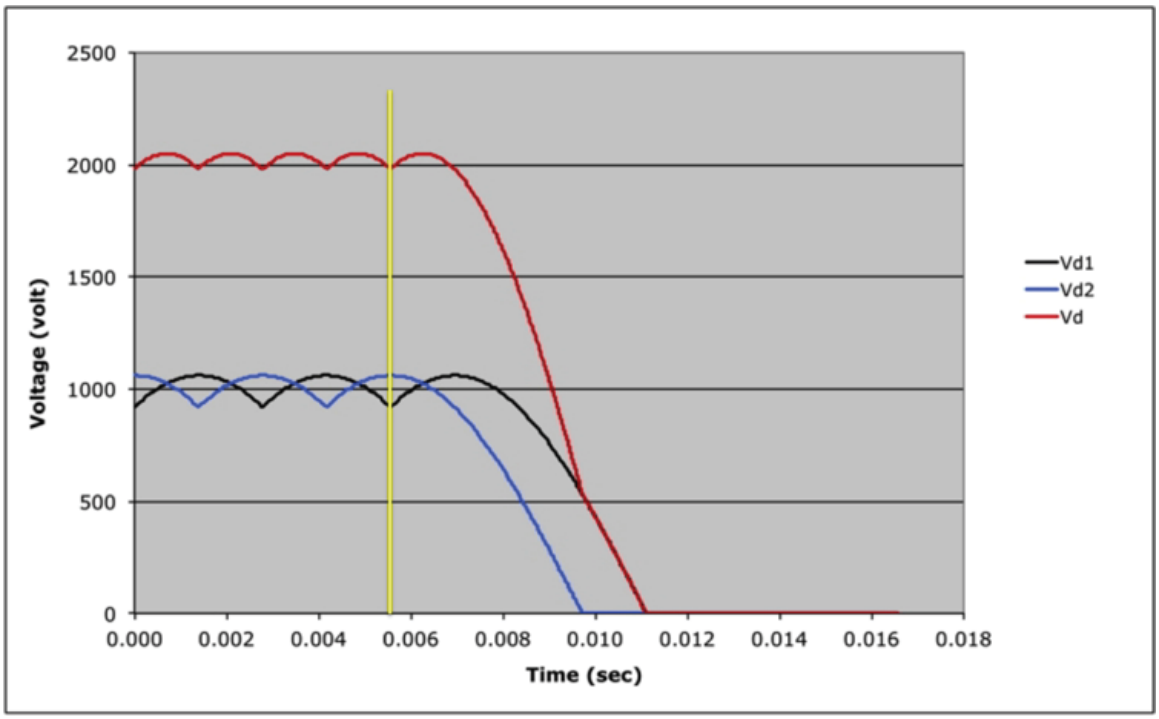


Figure 5 – Unipolar (PF1A) Suppress/Bypass Transient Voltage

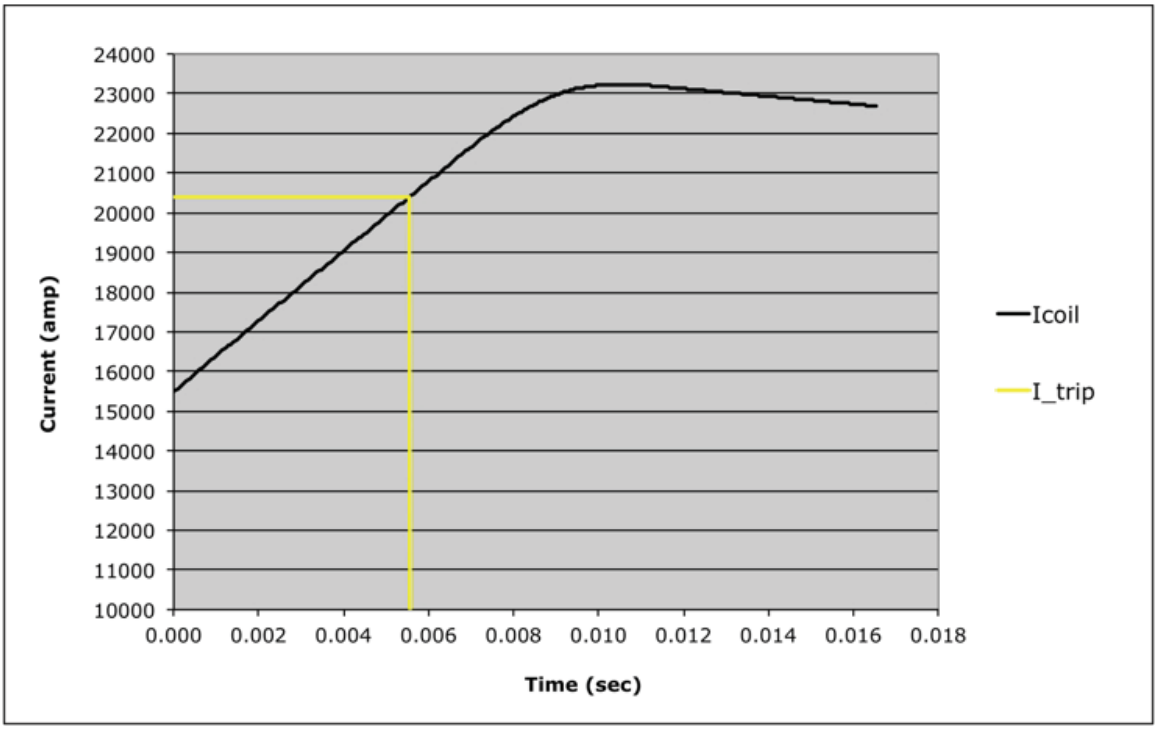


Figure 6 - Unipolar (PF1A) Suppress/Bypass Transient Current

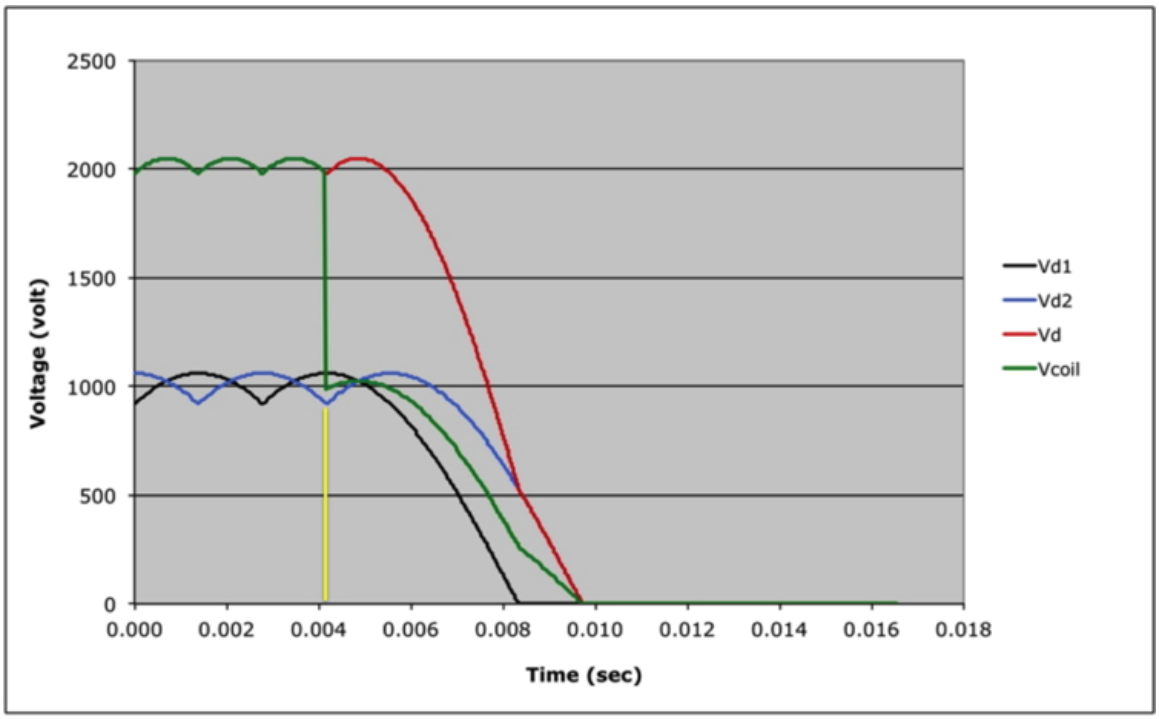


Figure 7 - Bipolar (PF1B) Suppress/Bypass Transient Voltage

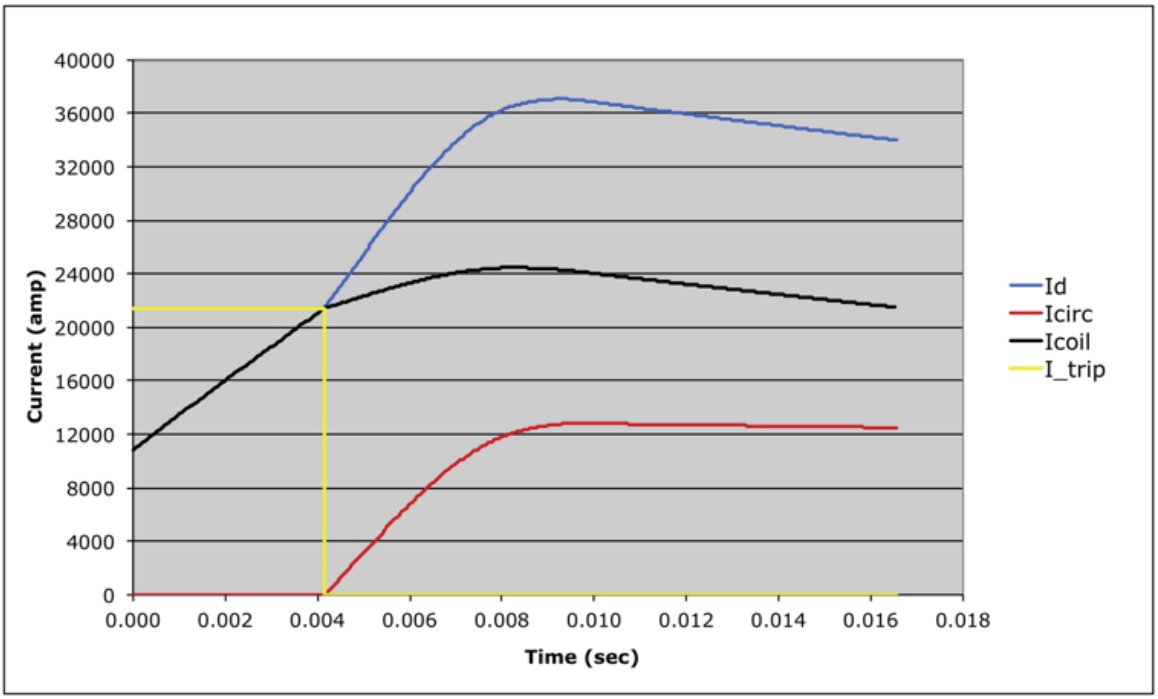


Figure 8 - Bipolar (PF1B) Suppress/Bypass Transient Current

4.4 Calculation summary

Results for 2% and 5% headroom cases are given in Table 1. Comparison between the entries for the approximate calculation (dI_blip ~ (V-I*R)*dt/L) and the XL solution (dI_blip) show that the results are close.

Table 1 – Suppress/Bypass Transient Cases

Coil	PF1A		PF1B		PF1C		
Irated	20000	20000	21000	21000	20000	20000	Amp
Headroom multiplier	1.02	1.05	1.02	1.05	1.02	1.05	
Itrip	20400	21000	21420	22050	20400	21000	Amp
Lcoil	1.84E-03	1.84E-03	4.45E-04	4.45E-04	4.57E-04	4.57E-04	Henry
Rcoil	5.93E-03	5.93E-03	9.19E-03	9.19E-03	4.49E-03	4.49E-03	Ohm
Lclr	2.72E-04	2.72E-04	2.72E-04	2.72E-04	2.72E-04	2.72E-04	Henry
Rclr	1.00E-03	1.00E-03	1.00E-03	1.00E-03	1.00E-03	1.00E-03	Ohm
Lext	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	Henry
Rext	2.00E-03	2.00E-03	2.00E-03	2.00E-03	2.00E-03	2.00E-03	Ohm
Ltot	2.11E-03	2.11E-03	7.17E-04	7.17E-04	7.29E-04	7.29E-04	Henry
Rtot	8.93E-03	8.93E-03	1.22E-02	1.22E-02	7.49E-03	7.49E-03	Ohm
dI_blip ~ (V-I*R)*dt/L	2851	2837	2882	2822	3660	3626	Amp
dI_blip	2843	2840	3027	2984	3668	3648	Amp
Imax	23243	23840	24447	25034	24068	24648	Amp
Probability	5.00E-04	5.00E-05	5.00E-04	5.00E-05	5.00E-04	5.00E-05	Per pulse
Number of Pulses over NSTX-U Lifetime	10	1	10	1	10	1	Pulses

5 Conclusion

The calculations presented herein provide conservative estimates of the peak Inner PF Coil currents in case of overcurrent trips as well as probability of occurrence. If additional inductance is added to the circuits to reduce ripple then the peak currents will be less than estimated herein.

Future work should use circuit simulation such as PSCAD to model in greater detail, and should consider cases where all OH and PF currents shut down simultaneously due to Level 1 fault with initial conditions based on 96 equilibria cases.