Systems Requirements Document for the FCPC New Fault Detector for the NSTX Upgrade Projects

Revision 0

(NSTX-SRD-5X-116-00)

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Note: This SRD has also been reviewed by: R Hatcher, J. Corl, Xin Zhao, Weigeo Que and G. Baker.

1. Overview

This proposal is to replace the existing fault detector and all associated CAMAC modules used in the existing Transrex power supplies. The new fault detector will consist of two independent sections, one for each rectifier section and a common communications section, see block diagram on page 10. The new unit will use all existing cables and connectors for existing signals, but can add new connectors for new signals, such as Ethernet communications. New signals can also be added to unused pins on the existing connectors. The new unit can use the existing DC voltages for power as long as it draws no more current from these lines than the existing unit uses. Optionally 110VAC can be supplied to the new fault detector for new internal power supplies.

2. General Specifications

2.1. Mechanical

The new fault detector shall be mounted in a standard 19" relay rack. The unit can be no larger than 12¼" high and 23½" deep. All connectors required for operation will be on the rear panel. Test and diagnostic connectors can be mounted to the front panel. The unit shall be designed to operate from 0ºC to 50ºC.

2.2. Analog Inputs

The analog inputs to the fault detector must have the following characteristics.

2.2.1. Input Voltage Range

- ±10.0 volt and ±0.200 volts

2.2.2. Input filtering to provide for proper Nyquist-Shannon sampling .

- 4kHz 5 pole low pass filter (Gaussian)
- 16 times oversampling when digitizing inputs with a decimation filter implemented.
- ±150 volt common mode voltage range
- 200kΩ input impedance
- One pole 2MHz RF filter
- 300 volt overvoltage on input without damage
- Programmable self test voltage for each analog input.
- 14 bit ADC with simultaneous sample and hold on all inputs
- All analog inputs differential and independent of each other
- Channel gain customization must not require tools.
- Gain and offset corrections applied in the digital processing chain.

2.3. DCCT

The existing FW Bell IF5004M DCCTs require 24 channels of independent current sources, one per DCCT. The nominal output current for each of these sources will be 40mA per channel. There shall be individual output enables for each channel. There will be individual status bit for each channel. All DCCT inputs must also have the option of optionally using a LEM LF2005-S or equivalent unit in place of any or all of the existing FW Bell units.

2.4. User Interface

2.4.1. Front Panel

The front panel display will be either a set of indicators (as on the current system) as well as a multi-line alpha-numeric display and associated keypad. Optionally a graphical display and keypad can be used where the indicators will be drawn on the display. In either case the display/keypad can be used to change parameters, with suitable protection (password/ key switch), run self-test routines, review system status and provide any other utility functions as they become needed. If a graphical display is included it would be useful to have the ability to view stored analog waveforms.

2.4.2. Web Server

Each fault detector will have a web server implemented, which will allow for monitoring of all signals and status indicators. The web server will not be able to change any settings.

2.4.3. EPICS Compatibility

The fault detector will be able to interface with the existing data acquisition system either as an EPICS server or as an EPICS IOC. In addition other communication protocols such as MODBUS/TCP can be implemented.

2.4.4. Configuration Files

All operational settings will be saved in one data file. This will allow for an easy setting of operational profiles.

2.4.5. Removable Storage

The fault detector will have some form of removable storage usable for data logging purposes as well as providing storage for software that may need to be installed in either the communications computer or firmware such as might be used in an FPGA.

2.4.6. Real World Values

All monitored points and limit settings must be in scaled engineering units.

2.5. Digital Inputs

All digital inputs will be optically isolated with a selectable input voltage. The maximum input current will be 7.4ma. The inputs will be switchable for a nominal 5V input (3.85V minimum) or a 12-24V input (10.5V minimum).

2.6. Analog Outputs

The analog outputs will be able to provide 250ma at ±10V with a 62.5Ω resistor provided in series with the output leg and the ground return leg.

2.7. Digital Outputs

2.7.1. Electrical Characteristics

The digital outputs will be able to source 24ma at greater than 4.5V and sink 24ma at less than 0.5V.

2.7.2. Fault Outputs

The fault outputs will toggle at a 1 milli second rate along with a clock signal. The exclusive OR of these two signals will be the actual fault signal. These signals will also be the inputs to watchdog timers, which will also be able to fault the system.

2.8. Monitoring and Data Storage

2.8.1. Limits

Trip levels will have fixed upper and lower values which can not be exceeded. Trip levels, offset and gain values will be stored with an overall CRC value. This will be checked periodically. Limits can only be changed after a suitable security protocol has been met, such as activating a key-switch or providing a password.

2.8.2. Internal Testing

All removable boards will have power supply voltage checks and board inserted checks.

2.8.3. Test Points

All input and output signals shall be available on easily accessed test points. These can be behind an easily opened panel.

2.8.4. Analog Value Storage

Analog signal storage: 4,194,304 word storage (16 bit words) for each section and for common signals. Each rectifier section is able to store 32 analog signals (18 ACCT, 12 DCCT, Input current, and output voltage) plus 2 auxiliary internal channels that can be assigned to internal signals in the FPGA under operator control. For the common signals there are eight analog signals (2 alpha inputs, 2 alpha limits and 2 primary voltages). This allows for 15.4 seconds of data recording with the starting point defined by the facility clock system. This will be expandable up to 16,777,216 words.

2.8.5. Change of State Storage

The fault detector will provide a 64 word FIFO with change of state input for fault storage, includes a 1μsecond resolution time stamp. Each word is 40 bits wide for the fault status and 24 bits wide for the time stamp.

2.9. Facility clock interface

The functions of a 404 timing module will be included in the fault detector. This shall be a two channel unit. This will be compatible with the existing 1MHz facility clock and the proposed 10MHz facility clock. It will have options for fiber-optic and twisted pair inputs and outputs.

3. Fault Detection Scenarios

Figure 1 below displays the fault detection scenarios.

TRANSREX PWR SUPPLY LIST OF FAULTS AND STATUS LIGHTS

CATEGORY	DESCRIPTION	DETECTION METHOD	DETECTION DEVICES	SCALE OF DEVICE	ADJUSTABLE RANGE
LEVEL 0 - Alarm Indication Only					
0A	Power module imbalance	|3-phase ACCT sum| > threshold	ACCT x 36	0.3125V per kA	0-1.76V / 0-3.38kA
0B	Bypass leg imbalance	Highest - Lowest > Threshold	DCCT x 24	50-100mV per kA	N/A
0C	Bypass leg fail to conduct	Bypass leg not conducting when Not(Block Bypass) and Vd < 0	DCCT x 24 and DCPT x 2	1.5V/KA	465A FIXED
0D	Firing Generator Not Ready	TBD	FG	N/A	N/A
0E	MGD PS OK	MGD box	MGD Box	N/A	N/A
0F	Loss of Cooling Water	Flow switch	Flow switch and timer	N/A	10 - 70 GPM
0G	PT failure	PT undervoltage relay	2 x UV relay	14400KV/120V	20V - 200V
LEVEL 1 - Suppress Power Modules, Fire Bypass Modules					
1A	Power Module Overcurrent	Any leg > trip level	ACCT x 36	0.3125V per kA	0-10.25V / 0-6.57ka
1B	Section Overcurrent	Id > trip level	Rectified secondary ACCT x 2	+30kA / +15V	2.5kA - 27.5kA
1C	Bypass Fail to Block	Any of bypass module currents greater than limit and no bypass command	DCCT x 24	50-100mV per kA	0.0kA - 1.0kA
1D	Loss of Cooling Water w/Permissive	Flow switch indicates for > adjustment time and Permissive	Flow switch and timer	N/A	10 - 70 GPM 0 - 10 seconds
1E	AC Ckt Breaker Advance Trip Signal	CB ADV trip coil enegized	Relay	N/A	N/A
1F	AC OV Suppressor Fuse Blown	AC suppressor Assembly / blown fuse	Microswitch	N/A	N/A
1G	Section Current Overtime	Id duration > overtime setting	Rectified secondary ACCT x 2	N/A	0 - 18sec
1H	Loss of AC w/o Ckt Brkr Advance Trip Signal	One or both PT undervoltage relays w/o Adv Trip	2 x UV relay	14400KV/120V	20V - 200V
1I	External Level 1 Fault	Descrete input	125VDC F1P and HCS input	N/A	N/A
1J	Permissive Sequence Fault	(Permissive)*(Fault Detector Not Ready)	logic	N/A	N/A
1K	DC power voltage error +24V, +15V, -15V, +5V	voltage>upper limit, voltage<lower limit		N/A	±5% - ±10%
1O	Loss of Command Link while Permissive On	(Link Not Ready)*(Permissive On)	Logic	N/A	N/A
1P	Loss of Permissive during Pulse	(Permissve Off)*(Convert On)	Logic	N/A	N/A
LEVEL 2 - Open AC Feeder Circuit Breaker					
2A	Failure to Suppress Firing	Any Power Module ACCT <> limit 1/2 cycle after suppression	ACCT x 36	0.3125V per kA	0.0kA - 1.0kA
LEVEL 3 - Suppress Power Modules, Fire Bypass Modules, Close DC Ground Switch					
3A	Bypass Leg Overcurrent	Bypass Leg Current > threshold	DCCT x 24	50-100mV per kA	0.0kA - 6.67kA
3B	All Bypass Fail to Conduct	Not(Bypass Block) + All Bypass Leg Current = 0 ….. Negative bridge voltage sensed after BB command issued	Voltage Xdcr	1V/150V	0 - 500V, 350V nominal
3C	External Level 3 Fault	Descrete input	125VDC F3P and HCS input	N/A	N/A

STATUS INDICATION

Signal	Quantity	Description
Permissive	1	Status of Permissive
Internal L1	1	Status of Internal Level 1 Fault Line
Internal L3	1	Status of Internal Level 3 Fault Line
External L1	1	Status of External Level 1 Fault Line
External L3	1	Status of External Level 3 Fault Line
Reset	1	Status of Reset
Command L	1	Status of input data command link
Convert Bit	2	Command input controlling gate pulses to power module thyristors
Bypass Bit	2	Command input controlling gate pulses to bypass module thyristors
CB Adv Trip	1	Status of Circuit Breaker Advance Trip Signal
AC PT	2	Status of PT undervoltage relays
Firing Gener	1	Status of Firing Generator
Cooling Wat	1	Status of flowmeter
MGD OK	4	Status of MGD Box
+24V OK	1	Status of local low voltage power supply
+15V OK	1	Status of local low voltage power supply
-15V OK	1	Status of local low voltage power supply
+5V OK	1	Status of local low voltage power supply

Figure 1 – Fault Detection Scenarios

4. Chassis connectors

Figure 2 below shows the current chassis connector pin assignments. Pins that go to the current CAMAC system are grayed out, and are currently not to be used.

Connector Pin	J37	J38	J39	J40	J41	J42
1	RESET card H - 16	ACCT CTA1A -	DCCT 1A out+		ACCT CTA1B-	DCCT 1B out+
2	PS PERM card H - 5	ACCT CTB1A -	DCCT 2A out+		ACCT CTB1B -	DCCT 2B out+
3	CB ADV card H - 11	ACCT CTC1A -	DCCT 3A out+	+15V in	ACCT CTC1B -	DCCT 3B out+
4	RESET +15V	ACCT CTA1A +	DCCT 1A in +		ACCT CTA1B +	DCCT 1B in +
5	PS PERM +15V	ACCT CTB1A +	DCCT 2A in +		ACCT CTB1B +	DCCT 2B in +
7	CB ADV +15V	ACCT CTC1A +	DCCT 3A in +	+15V in	ACCT CTC1B +	DCCT 3B in +
8	RESET gnd	ACCT CTA1A gnd	DCCT 1A out -	I sect A + in card M-1	ACCT CTA1B gnd	DCCT 1B out -
10	PS PERM gnd	ACCT CTB1A gnd	DCCT 2A out -	I sect B + in card M-2	ACCT CTB1B gnd	DCCT 2B out -
11	CB ADV gnd	ACCT CTC1A gnd	DCCT 3A out -	+15V in	ACCT CTC1B gnd	DCCT 3B out -
12	L O AC card H - 9	alpha 2 from FG	DCCT 1A in -	I sect A - in card M-M		DCCT 1B in -
13	PT FAIL card L - 15		DCCT 2A in -	I sect B - in card M-12		DCCT 2B in -
14	CICADA RDY H - 6		DCCT 3A in -	+15V in		DCCT 3B in -
15	L O AC +15V	ACCT CTA2A -	DCCT 1A gnd	+15V	ACCT CTA2B -	DCCT 1B gnd
16	PT FAIL +15V	ACCT CTB2A -	DCCT 2A gnd	+15V	ACCT CTB2B -	DCCT 2B gnd
17	CICADA RDY +15V	ACCT CTC2A -	DCCT 3A gnd	+15V	ACCT CTC2B -	DCCT 3B gnd
18	L O AC gnd	ACCT CTA2A +	DCCT 1A gnd	card I - D FD ready*	ACCT CTA2B +	DCCT 1B gnd
20	PT FAIL gnd	ACCT CTB2A +	DCCT 2A gnd	card I - C Level 1 fault	ACCT CTB2B +	DCCT 2B gnd
21	CICADA RDY gnd	ACCT CTC2A +	DCCT 3A gnd	card I - B CB Trip	ACCT CTC2B +	DCCT 3B gnd
22	120V card N - 3	ACCT CTA2A gnd	DCCT 4A out+	+15V	ACCT CTA2B gnd	DCCT 4B out+
23	WATER card H - 12	ACCT CTB2A gnd	DCCT 5A out+	+15V	ACCT CTB2B gnd	DCCT 5B out+
24	WATER2 card H - 15	ACCT CTC2A gnd	DCCT 6A out+	+15V	ACCT CTC2B gnd	DCCT 6B out+
25	120V +15V		DCCT 4A in +	card I - E Level 3 fault		DCCT 4B in +
26	WATER +15V		DCCT 5A in +	card I - F Mod OC*		DCCT 5B in +
27	WATER2 +15V		DCCT 6A in +	card I - H CB advance trip*		DCCT 6B in +
28	120V gnd	ACCT CTA3A -	DCCT 4A out -	+15V	ACCT CTA3B -	DCCT 4B out -
29	WATER gnd	ACCT CTB3A -	DCCT 5A out -	+15V	ACCT CTB3B -	DCCT 5B out -
30	WATER2 gnd	ACCT CTC3A -	DCCT 6A out -	+15V	ACCT CTC3B -	DCCT 6B out -
31	AC SUPR card H - 7	ACCT CTA3A +	DCCT 4A in -	card I - P CICADA ready	ACCT CTA3B +	DCCT 4B in -
32	MGD OK card L - J	ACCT CTB3A +	DCCT 5A in -	card I - N PS permissive	ACCT CTB3B +	DCCT 5B in -
33	LEVEL 1 in card G - 4	ACCT CTC3A +	DCCT 6A in -	card I - M Loss Water	ACCT CTC3B +	DCCT 6B in -
34	AC SUPR +15V	ACCT CTA3A gnd	DCCT 4A gnd	+15V	ACCT CTA3B gnd	DCCT 4B gnd
35	MGD OK +15V	ACCT CTB3A gnd	DCCT 5A gnd	+15V	ACCT CTB3B gnd	DCCT 5B gnd
36	LEVEL 1 in +15V	ACCT CTC3A gnd	DCCT 6A gnd	+15V	ACCT CTC3B gnd	DCCT 6B gnd
37	AC SUPR gnd		DCCT 4A gnd	card I - L FG ready		DCCT 4B gnd
38	MGD OK gnd		DCCT 5A gnd	card I - K AC supress fail		DCCT 5B gnd
39	LEVEL 1 in gnd		DCCT 6A gnd	card I - J I overtime*		DCCT 6B gnd
40	LEVEL 3 in card G - 3	ACCT CTA4A -	DCCT 7A gnd	+15V	ACCT CTA4B -	DCCT 7B gnd
41	LEVEL 1 out card G - K	ACCT CTB4A -	DCCT 8A gnd	+15V	ACCT CTB4B -	DCCT 8B gnd
42	LEVEL 3 out card G-R	ACCT CTC4A -	DCCT 9A gnd	gnd in	ACCT CTC4B -	DCCT 9B gnd
43	LEVEL 3 in +15V	ACCT CTA4A +	DCCT 7A gnd	card I - T Bypass fail*	ACCT CTA4B +	DCCT 7B gnd
44	~SUPPR card G - N	ACCT CTB4A +	DCCT 8A gnd	card I - V Bypass rev.*	ACCT CTB4B +	DCCT 8B gnd
45	OPEN CB card G - X	ACCT CTC4A +	DCCT 9A gnd	gnd in	ACCT CTC4B +	DCCT 9B gnd
46	LEVEL 3 in gnd	ACCT CTA4A gnd	DCCT 7A out+	+15V	ACCT CTA4B gnd	DCCT 7B out+
47	LEVEL 1 out gnd	ACCT CTB4A gnd	DCCT 8A out+	+15V	ACCT CTB4B gnd	DCCT 8B out+
48	LEVEL 3 out gnd	ACCT CTC4A gnd	DCCT 9A out+	gnd in	ACCT CTC4B gnd	DCCT 9B out+
49	SUPP BP card G - L		DCCT 7A in +	card I - U Bypass OC		DCCT 7B in +
50	gnd		DCCT 8A in +	card I - S Bypass fail to conduct		DCCT 8B in +
51	OPEN CB gnd		DCCT 9A in +	gnd in		DCCT 9B in +
52	SUPP BP card O - J	ACCT CTA5A -	DCCT 7A out -		ACCT CTA5B -	DCCT 7B out -
53	gnd (stp 55,56)	ACCT CTB5A -	DCCT 8A out -		ACCT CTB5B -	DCCT 8B out -
54	AC ON card H - A	ACCT CTC5A -	DCCT 9A out -	gnd in	ACCT CTC5B -	DCCT 9B out -
55	Id ret	ACCT CTA5A +	DCCT 7A in -		ACCT CTA5B +	DCCT 7B in -
56	Id card M - 11	ACCT CTB5A +	DCCT 8A in -		ACCT CTB5B +	DCCT 8B in -
57	~INV LIMIT card H - 13	ACCT CTC5A +	DCCT 9A in -	gnd in	ACCT CTC5B +	DCCT 9B in -
58		ACCT CTA5A gnd	DCCT 10A gnd	I sect A out gnd	ACCT CTA5B gnd	DCCT 10B gnd
59		ACCT CTB5A gnd	DCCT 11A gnd		ACCT CTB5B gnd	DCCT 11B gnd
60		ACCT CTC5A gnd	DCCT 12A gnd		ACCT CTC5B gnd	DCCT 12B gnd
62	gnd (twp w 63)		DCCT 10A gnd	I sect A out card M-10		DCCT 10B gnd
63	Id>0 card M - 6		DCCT 11A gnd			DCCT 11B gnd
64	BP Block card L - S		DCCT 12A gnd	B voltage out		DCCT 12B gnd
65	FG READY card I - 14	ACCT CTA6A -	DCCT 10A out+	I sect B out card M-9	ACCT CTA6B -	DCCT 10B out+
66	SUPRESS card N - L	ACCT CTB6A -	DCCT 11A out+	A voltage out	ACCT CTB6B -	DCCT 11B out+
67	CYCLIC bypass	ACCT CTC6A -	DCCT 12A out+	gnd (twp w 64)	ACCT CTC6B -	DCCT 12B out+
70		ACCT CTA6A +	DCCT 10A in +	Pri CT3 in +	ACCT CTA6B +	DCCT 10B in +
71		ACCT CTB6A +	DCCT 11A in +	I sect B out gnd	ACCT CTB6B +	DCCT 11B in +
72		ACCT CTC6A +	DCCT 12A in +	-15V in	ACCT CTC6B +	DCCT 12B in +
73		ACCT CTA6A gnd	DCCT 10A out -	Pri CT3 in -	ACCT CTA6B gnd	DCCT 10B out -
74		ACCT CTB6A gnd	DCCT 11A out -	gnd (twp w 66)	ACCT CTB6B gnd	DCCT 11B out -
75		ACCT CTC6A gnd	DCCT 12A out -	-15V in	ACCT CTC6B gnd	DCCT 12B out -
76			DCCT 10A in -	Pri CT1 in +		DCCT 10B in -
77			DCCT 11A in -	Pri CT2 in +		DCCT 11B in -
78		gnd (twp w 82)	DCCT 12A in -	-15V in	gnd (twp w 82)	DCCT 12B in -
79				Pri CT1 in -		
80				Pri CT2 in -		
82		A voltage card O - A		-15V in	B voltage card O - 9	

Figure 2 – Chassis Connectors

The existing connectors are shown in the following drawing (Figure 3), and will be used for exiting signals used by the new system.

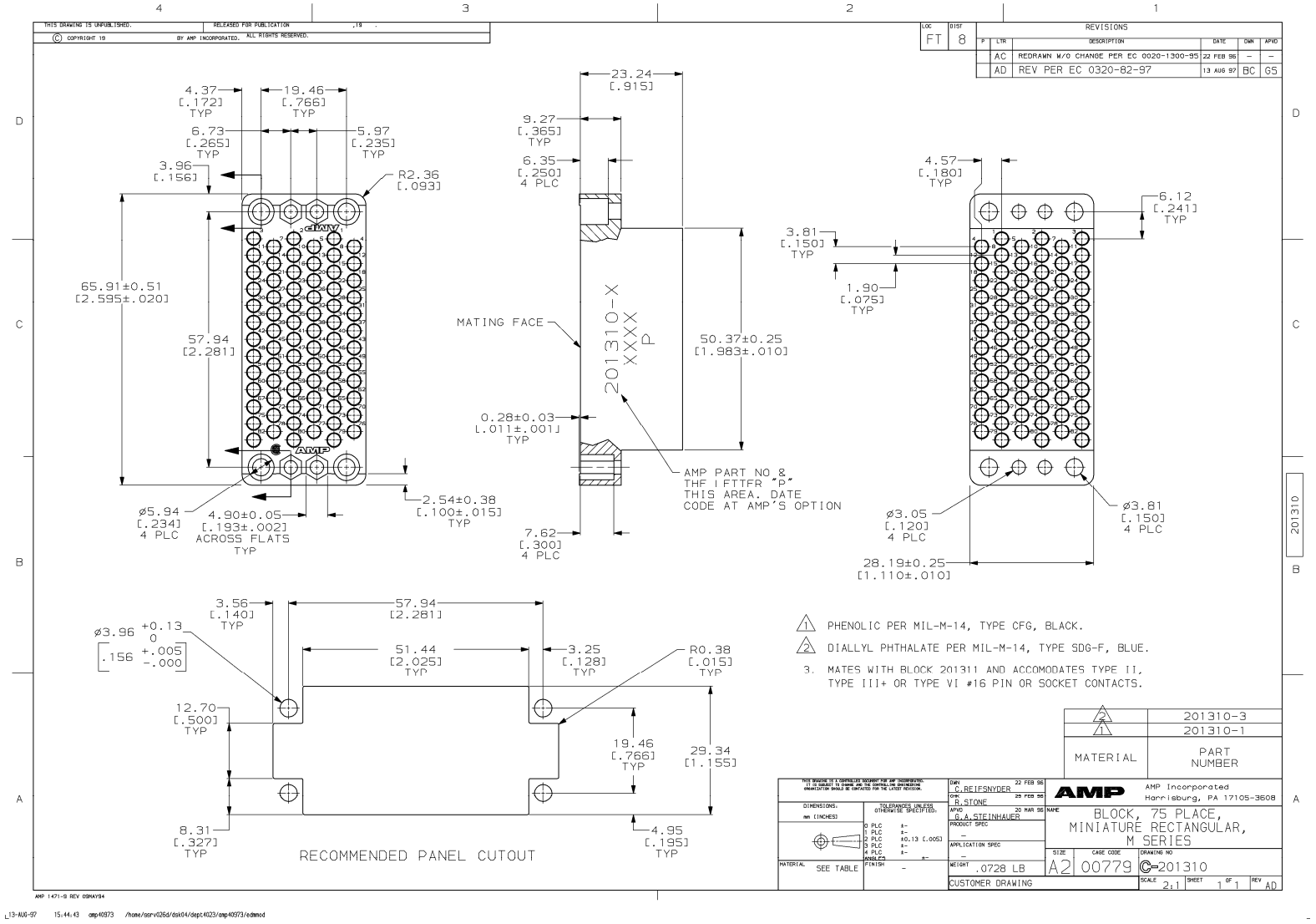

Figure 3 – Existing Connectors

5. Simplified Block Diagram

Figure 4 below shows a simplified block diagram of the new fault detector.

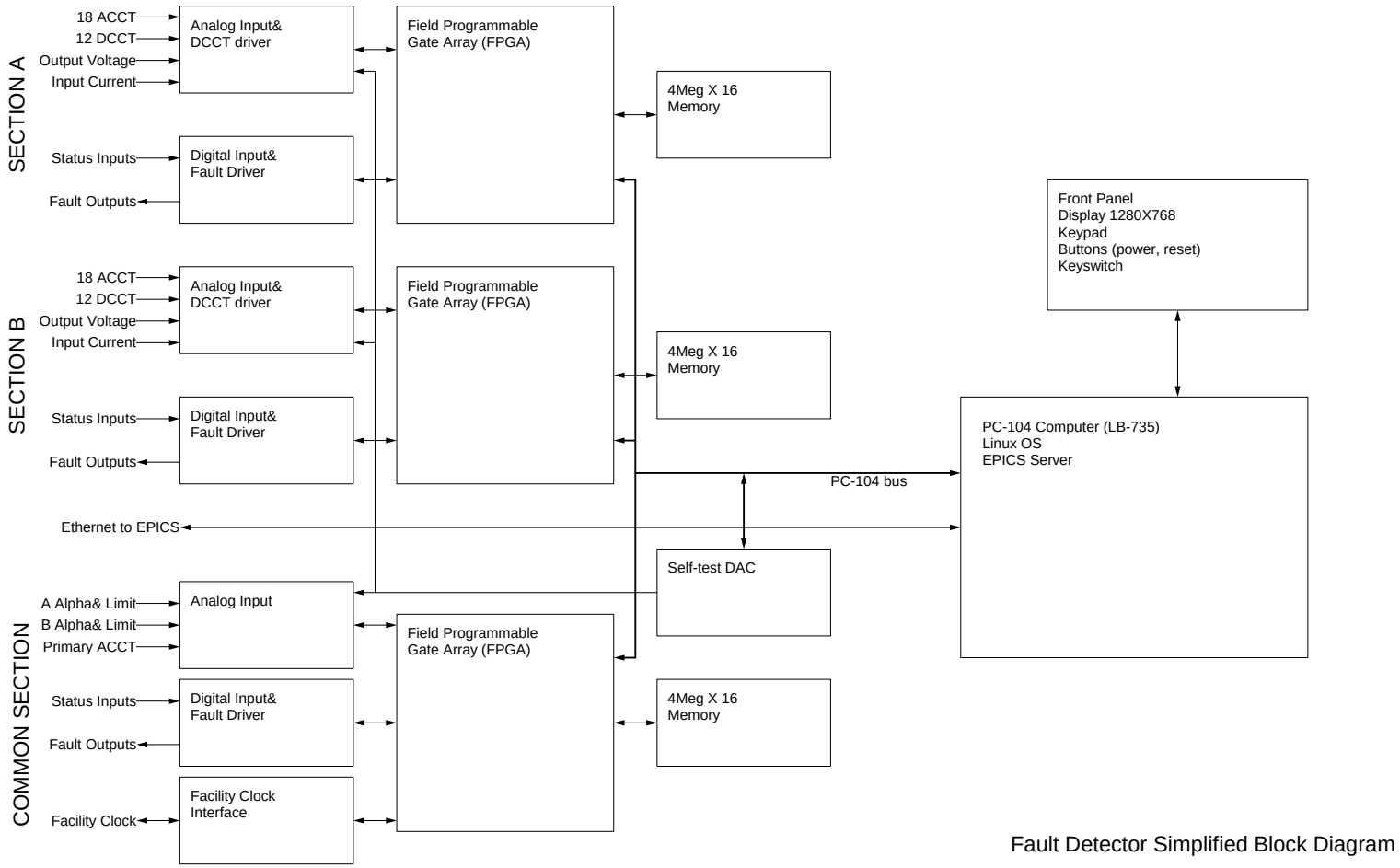

Figure 4 - Simplified Block Diagram of the New Fault Detector