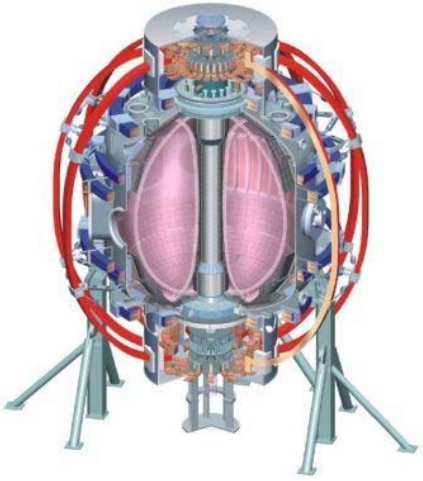
Power System

Raki Ramakrishnan (WBS5 Manager)

Weiguo Que: Cog Engineer (Analysis)

Xin Zhao: Cog Engineer (Controls)

NSTX Center Stack Upgrade Peer Review
LSB B318
May 18, 2011



- Columbia U
- CompX
- General Atomics
- FIU
- INL
- Johns Hopkins U
- LANL
- LLNL
- Lodestar
- MIT
- Nova Photonics
- New York U
- ORNL
- PPPL
- Princeton U
- Purdue U
- SNL
- Think Tank, Inc.
- UC Davis
- UC Irvine
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- U Colorado
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- Culham Sci Ctr
- U St. Andrews
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- Chubu U
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- NIFS
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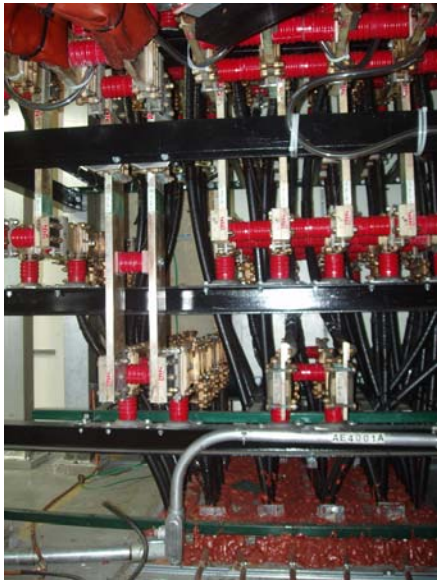
- JAEA
- Hebrew U
- Ioffe Inst
- RRC Kurchatov Inst
- TRINITI
- NFRI
- KAIST
- POSTECH
- ASIPP
- ENEA, Frascati
- CEA, Cadarache
- IPP, Jülich
- IPP, Garching
- ASCR, Czech Rep

PWR SYSTEM UPGRADE FOR NEW CENTER STACK

- REQUIREMENTS
- TF : 129.8 kA, 1kV, ESW 7.08 sec every 2400 sec (7.05kA rms) ;
- OH : 24kA, ESW *1.474* sec every 2400 sec ; 6kV
- PF1a: Eliminate Ripple reduction reactors
- Other PF : Existing config. meets requirements for other PF

- CONSTRAINTS:
- Constraints analyzed to project realistic estimate
  - NSTX machine is located in NTC - is small in area.
  - Constrained space in the basement of NTC
  - FCPC Building has limited space & equipment is virtually crammed inside. No basement in this building.
  - Thus real estate availability is very limited and design of upgrades has to meet these limitations
  - TF has now four parallels. Thus short circuit current about 250kA. Upgrade dictates doubling parallels - short circuit current also gets doubled – the forces are four times more. Hence power loop components require appropriate upgrade. Also additional protective measures are required.

Pwr. System Equipment



NSTX Upgrade Coil Ckt. Summary

NSTX Coil Circuits Summary for Upgrade												
Coil Ckt. #	NSTX Coil	ESW Pulse duration (Sec)	Pulse Period (Sec)	Pulse Period Ultimate (Sec)	Bipolar OR Unipolar	# of branches	Voltage (kV)	ESW Current Fwd. (kA)	ESW Current Rev (kA)	RMS Coil Current AMPS	RMS Coil Current Ultimate AMPS	Comments
1	**TF**	**7.08**	**2400**	**1200**	**U**	**8**	**1**	**130**	**0**	**7061**	**9985**	**Increased current**
2	OH	1.474	2400	1200	B	2	6	24	-24	595	841	**Change CLR**
3	PF1aU	5.5	2400	1200	B	2	1	18	-7	862	1219	**Eliminate ripple reactor**
4	PF1aL	5.5	2400	1200	B	2	1	18	-7	862	1219	**Eliminate ripple reactor**
5	PF1bU	2.104	2400	1200	U	1	1	13	0	385	544	Not powered
6	PF1bL	2.104	2400	1200	U	1	1	13	0	385	544	No Change
7	PF1cU	4.341	2400	1200	U	1	1	16	0	680	962	Not powered
8	PF1cL	4.341	2400	1200	U	1	1	16	0	680	962	Not powered
9	PF2U	5.5	2400	1200	U	1	1	15	-11	718	1016	No Change
10	PF2L	5.5	2400	1200	U	1	1	15	-11	718	1016	No Change
11	PF3U	5.5	2400	1200	B	2	2	12	-16	766	1083	No Change
12	PF3L	5.5	2400	1200	B	2	2	12	-16	766	1083	No Change
13	PF4	5.5	2400	1200	U	1	2	16	0	766	1083	No Change
14	PF5	5.5	2400	1200	U	1	3	24	0	1149	1625	No Change
15	RWM	5.5	2400	1200	B	1	1	3.3	3.3	158	223	No Change

TF POWER LOOP DESIGN

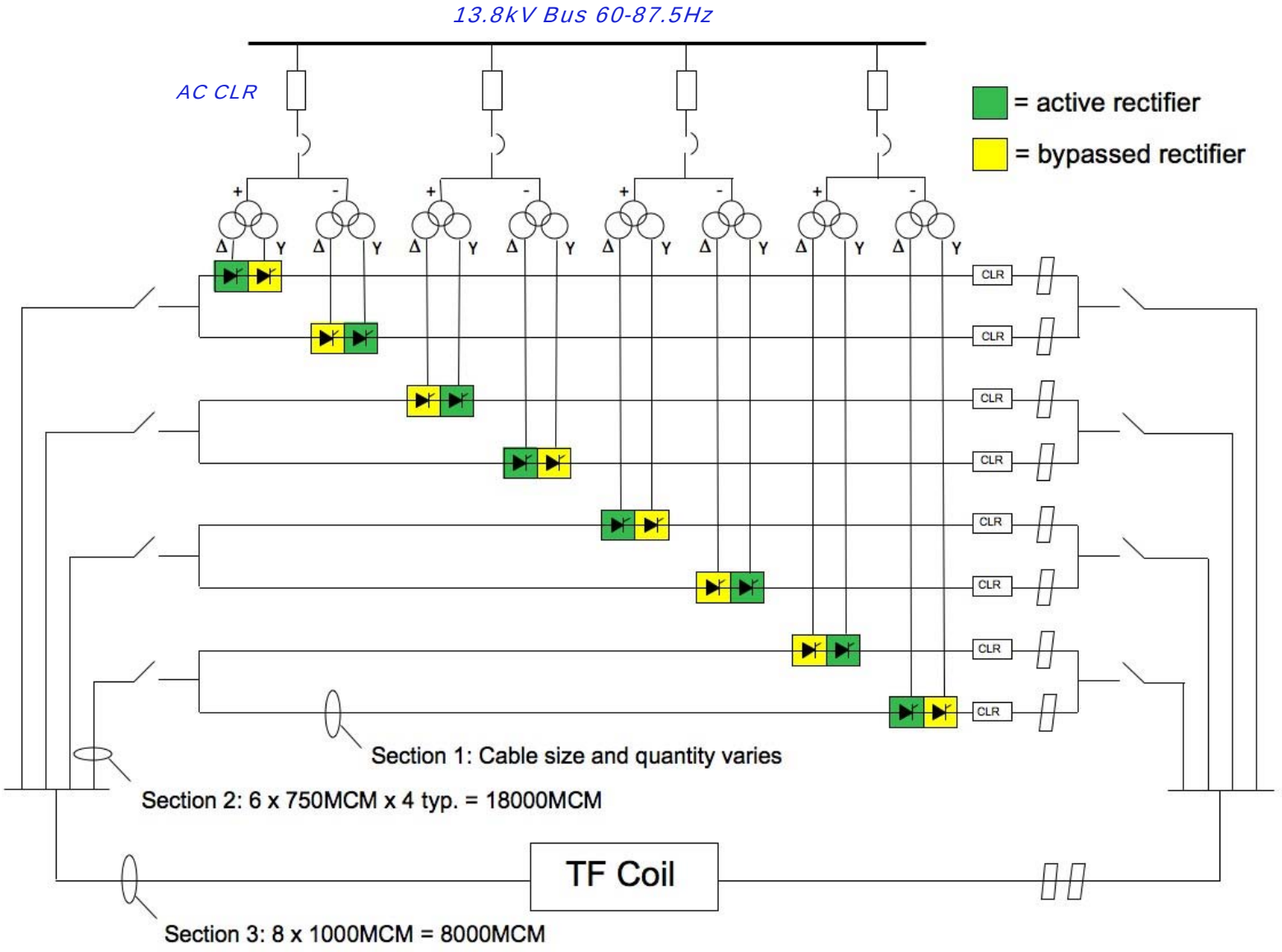
- **Four additional PARALLELS of Transrex power supplies to be provided to existing four parallels**
- **Each parallel - two 1 kV Transrex power supply sections in series.**
  - **CLRs will be connected between the supplies**
  - **One section of the supply will be used as a Diode**
- **Existing four SDS of TF with additional parallel supplies will be used.**
  - **two parallels to be fed via each switch.**
- **Four more DC reactors (270uH) to be used in the additional 4 parallels.**
  - **Since upgraded OH circuit needs reactors of higher inductance, the existing 270uH OH CLRs will be reconnected in the TF Circuit.**
- **To install reactors in TF wing**
  - **(1) Remove PF1a Ripple reduction Reactors & store; and**
  - **(2) Remove four CICADA Racks in the middle of isle.**

TF POWER LOOP DESIGN – Contd.

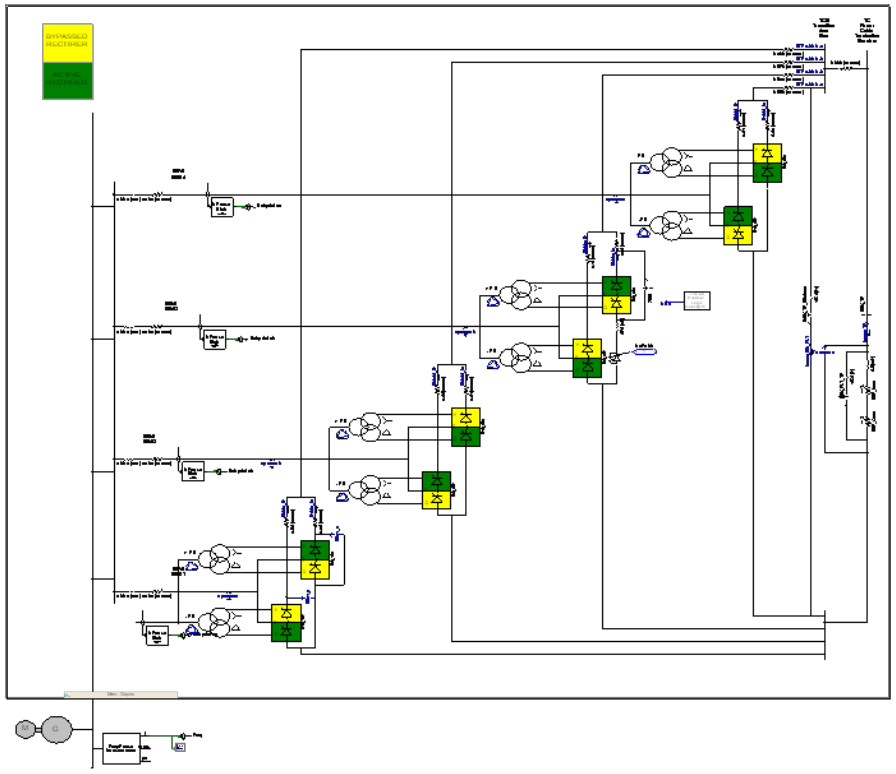
- **DCCTs**
  - Existing eight DCCTs will be repositioned to detect current in each of the eight parallels
  - Eight additional DCCTs will be purchased and installed
  - Two new DCCTs to detect total TF Coil Current
  - The Vacuum Control Room presently empty will be used for housing the electronics boxes
- **CABLING**
  - Reconnect existing cabling as needed.
  - Install additional power cabling within FCPC - nearly ***7000*** feet of 1000mcm 5kV power cables. Limited space makes bus installation difficult
  - Reconnect existing power cabling in Transition Area (TA) - in TFTR Test Cell Basement- to NSTX Test Cell for TF use.
  - Provide Control Cabling as needed

- **Modify Power Cable Termination Structure (PCTS) for TF to handle fault currents & to accept 3 more power cables/pole.**

TF Feed – One line diagram



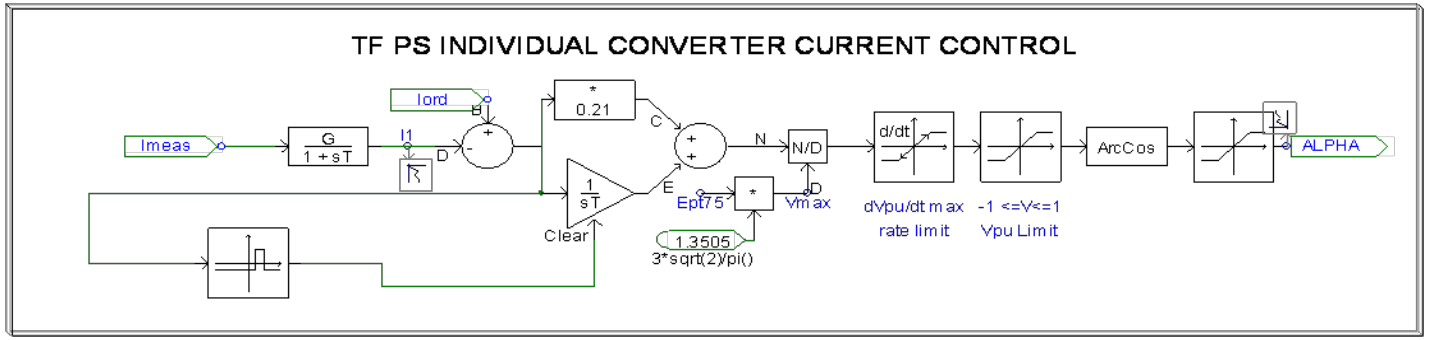
PSCAD ANALYSIS Simulation Model (Weiguo Que)



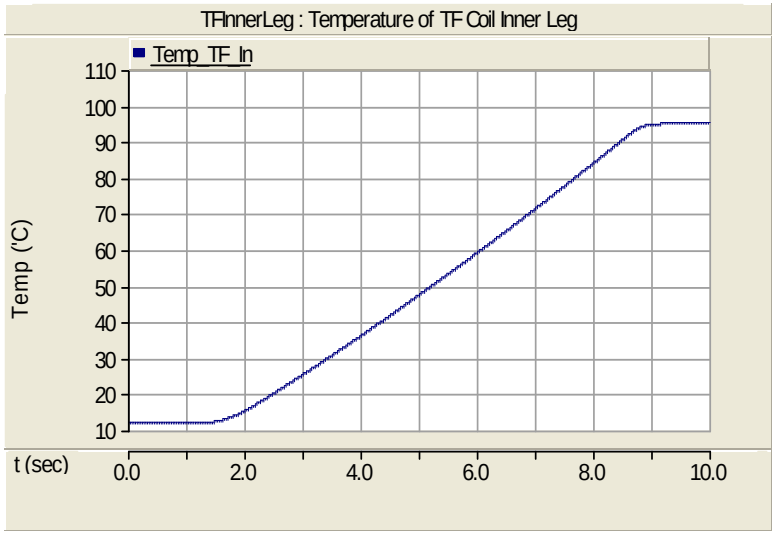
- Eight power supply branches are used and the control algorithm will control the converter firing angle alpha such that the current in each branch is 1/8 of the total TF coil current. Each power supply has its own PI current controller.

- PI Current Controller :
  - Proportional gain: K=0.21
  - Integrator Time Constant: 3 second applied when I error falls below 6.5 kA.

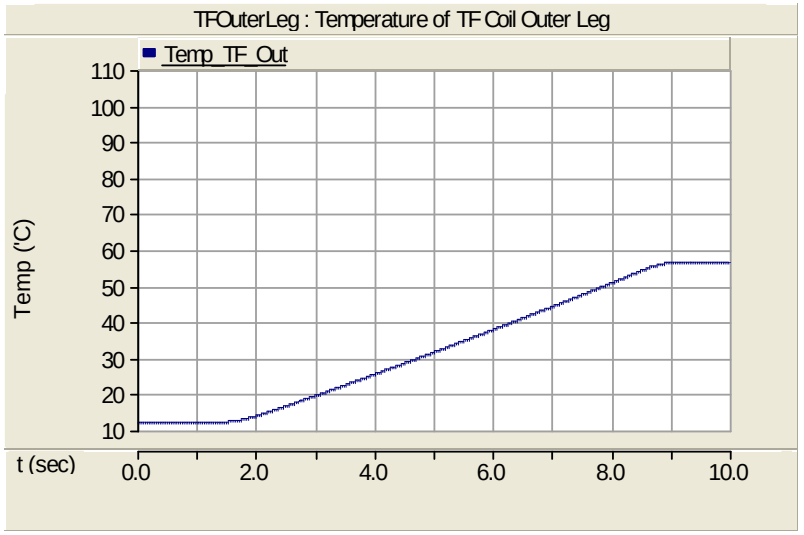
- Over Current Trip: 22 kA, block and bypass with 10 msec delay.



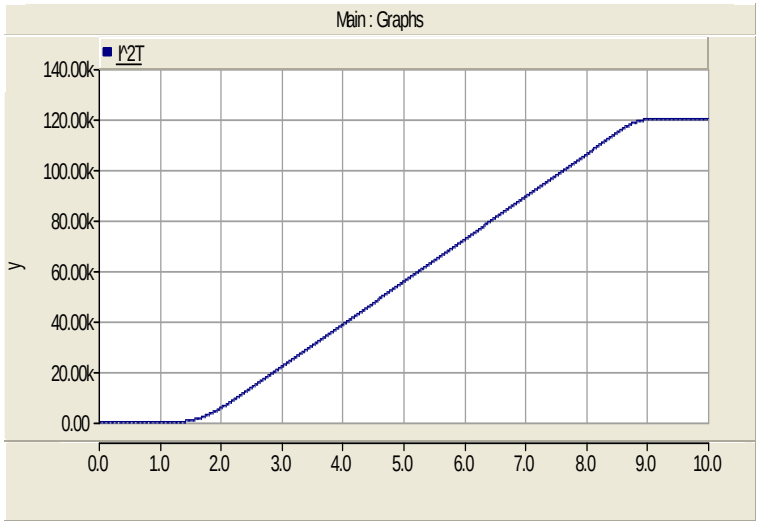
PSCAD ANALYSIS Simulation Results (Weiguo Que)



TF Coil Inner Leg Temperature



TF Coil Outer Leg Temperature



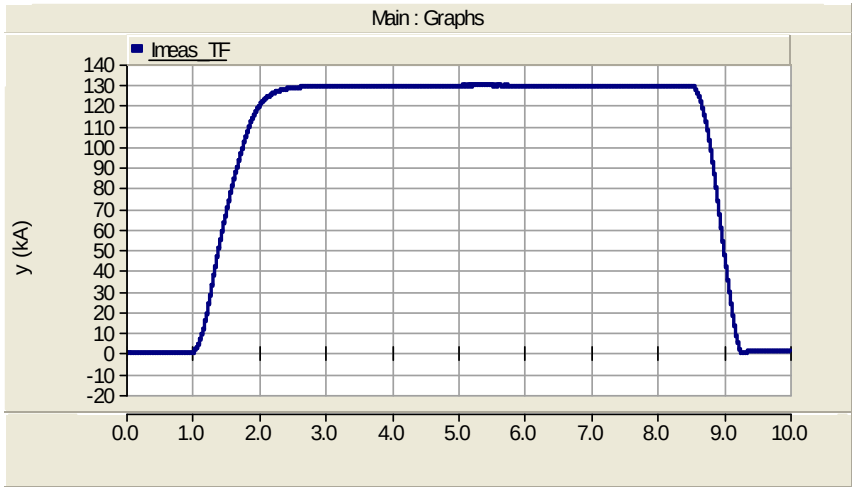
I^2t Calculation

TF Coil Inner Leg Temperature:
Rise From 12 degree C To 94.9 degree C

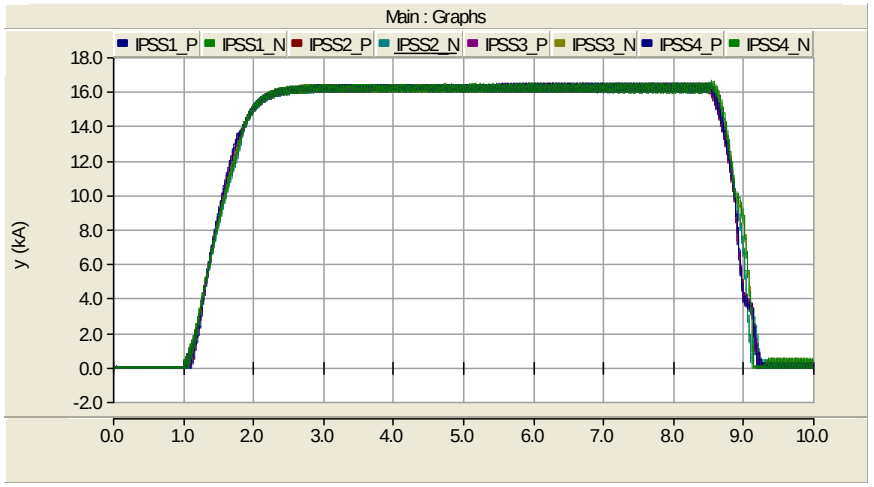
TF Coil Outer Leg Temperature:
Rise From 12 degree C To 56.4 degree C

I^2t: Simulation: 1.2007E+5 (kA*kA*Sec)
Theory: 1.1965E+5 (kA*kA*Sec)

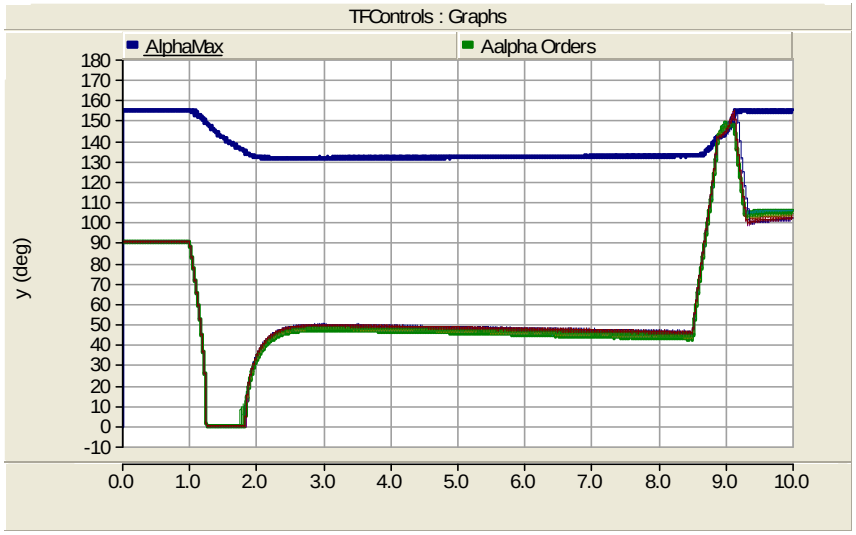
PSCAD ANALYSIS Normal Work Condition (Weiguo Que)



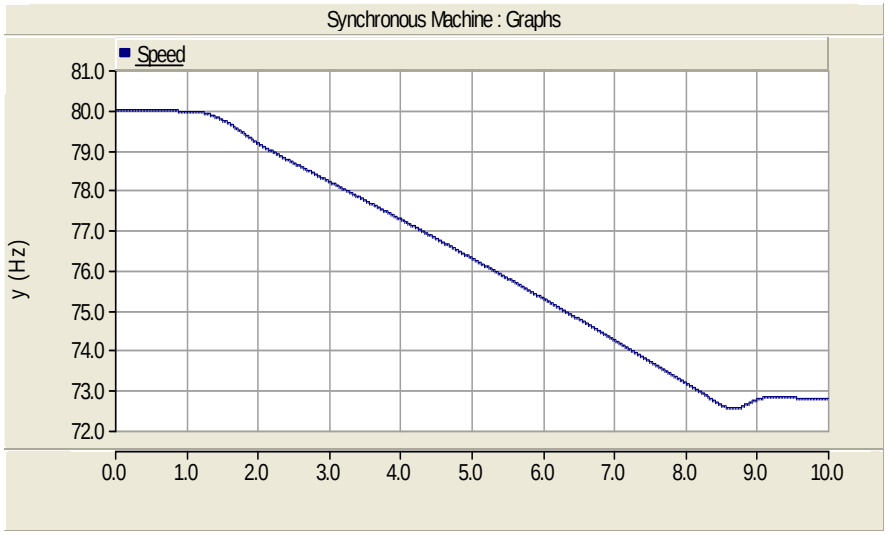
TF coil current 130 kA, 6.5 second



Power Supply Branch current 16.25 kA



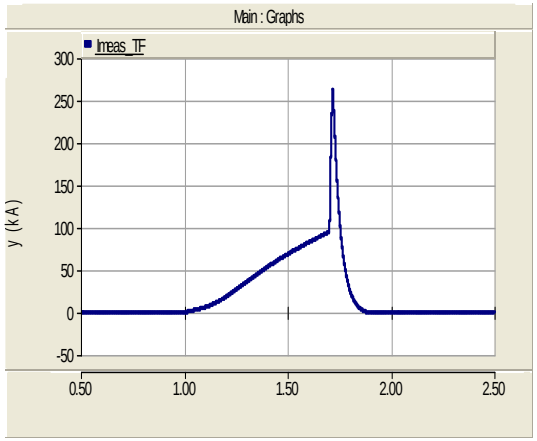
Alpha angle control and alpha limits calculation



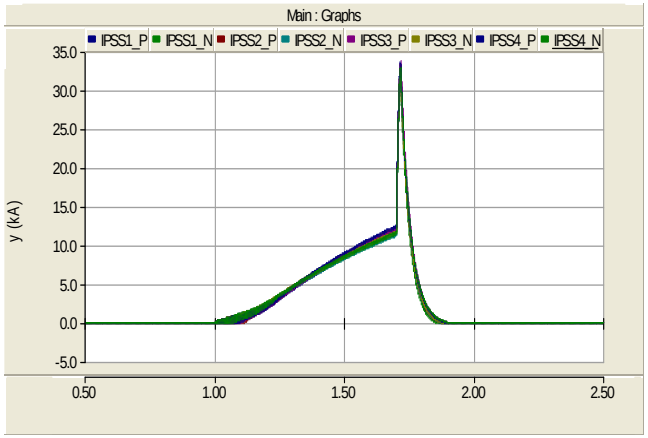
Motor-Generator Speed

PSCAD ANALYSIS TF coil and Disconnect Switch Short Circuit Condition (Weiguo Que)

Case 1: TF Coil Short Circuit



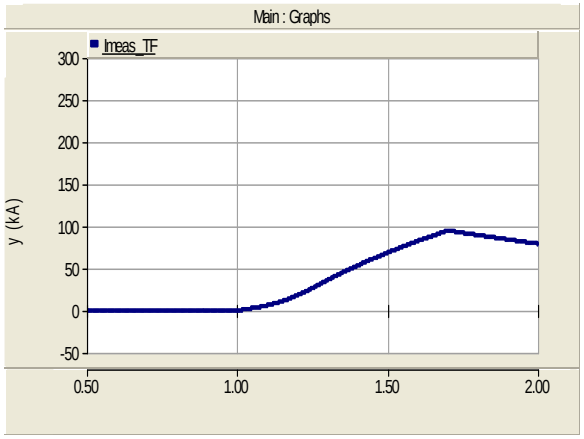
TF coil short circuit current 1.7 sec



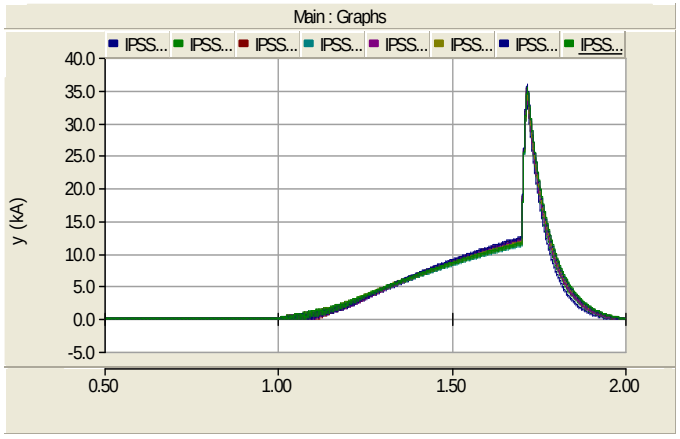
Branch short circuit current 1.7 sec

Time (sec)	TF Coil Short Branch Max. Current(kA)	TF Coil Short Circuit Current (kA)
1.2	28.1	219.4
1.4	33.9	262.4
1.5	33.7	262.9
1.6	34.4	263.1
1.7	33.8	263.4
1.8	33.6	262.2
1.9	31.3	242.7
2	28.8	225.8
3	25.4	199.9
8	26.9	211.5
8.6	16.4	126.1

Case 2: Disconnect Switch Short Circuit



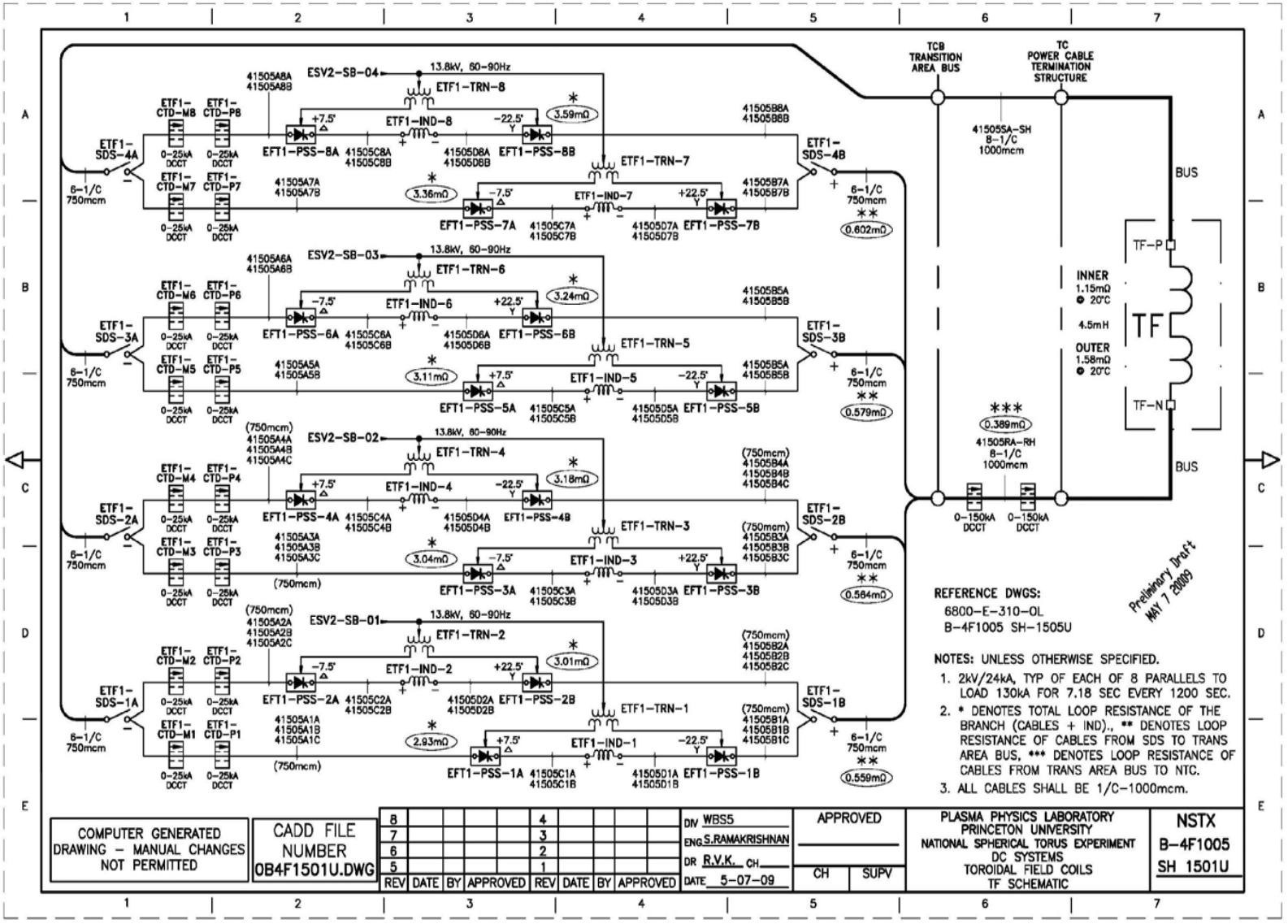
TF coil short circuit current 1.7 sec



Branch short circuit current 1.7 sec

Time (sec)	Disconnect Switch Short Branch Max. Current(kA)
1.2	30.6
1.4	35.5
1.5	35.5
1.6	35.6
1.7	35.9
1.8	35.9
1.9	33.1
2	31.6
3	27.8
8	29.1
8.6	17.4

TF CIRCUIT – 129.8kA, 1kV (8 parallels)



OH PWR. LOOP DESIGN & PF PWR. LOOP DESIGN BASIS

EXISTING OH PWR LOOP DESIGN:

- 6kV Anti-parallel configuration
- 24kA for 0.4 seconds every 600 seconds

UPGRADE - OH PWR LOOP DESIGN:

- 6kV Anti-parallel configuration
- 24kA for 1.474 sec every 2400 seconds

Work Required

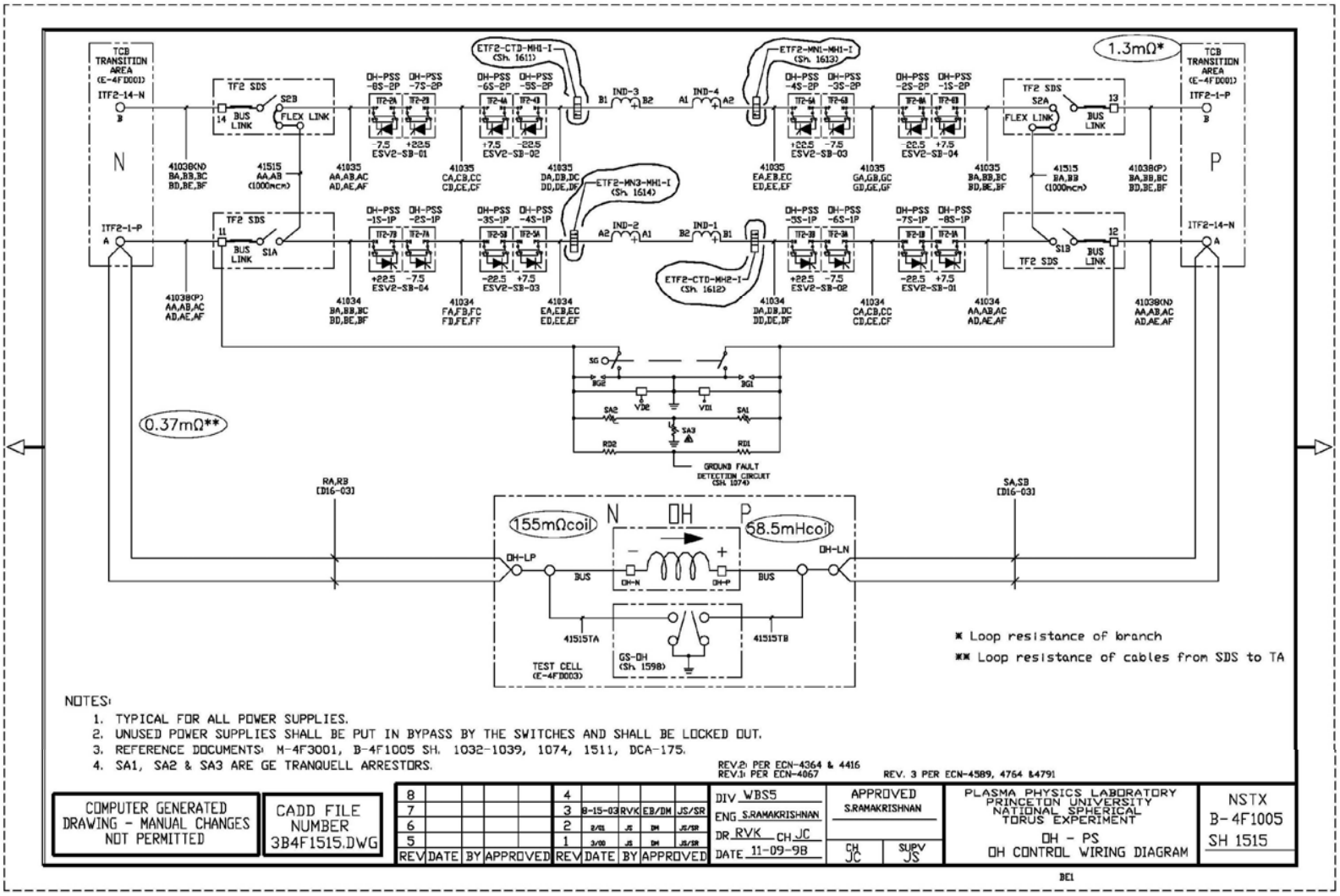
- The DC CLR values have been optimized to the new requirement based on PSCAD analysis. These new reactors of the required values will be purchased and installed.
- All the other equipment and cabling in the power loop will be used AS IS

PF COILS

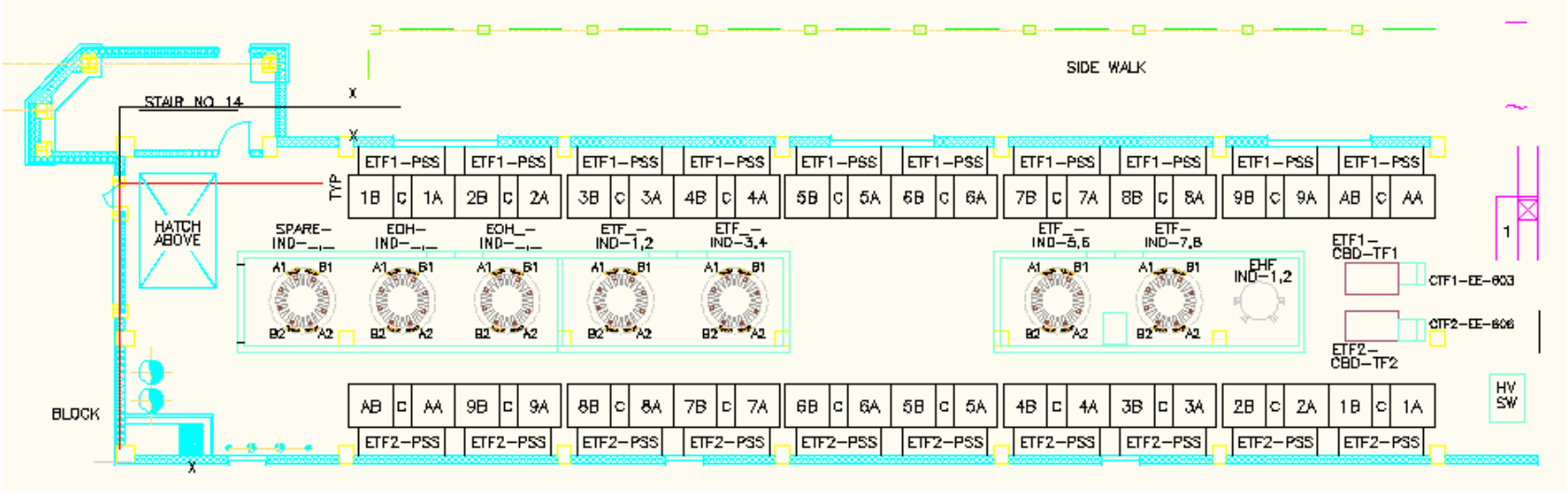
PF DESIGN:

- Existing circuits for PF1b, PF2, PF3, PF4,and PF5 will be used AS IS for the upgrade.
- PF1a Changes
  - The ripple reduction reactors in the PF1aU & PF1aL circuits will be eliminated based on the newly designed PF1a Coils
  - Associated power cabling changes will be made.

OH CIRCUIT – ANTI-PARALLEL 6kV;+/-24kA



FCPC BLDG. TF WING - REACTOR LAYOUT



CONTROL & PROTECTION

- CONTROLS
  - Hardwired Controls will be upgraded
- CIRCUIT PROTECTION
  - Analog Coil Protection Units (ACPs) will be modified as needed
- RECTIFIER PROTECTION
  - ACCT, DCCT & PT signals along with other interlocks will be processed in the FD. See Block diagram.
  - Fault Detector (FD) in Rectifiers
    - Overcurrent
    - Pulse duration
  - FD will generate Level 1, 2, 3 faults to trip.

- Digital Coil Protection (DCP):
  - DCP is designed for protecting the machine support system.

- DCP design will be presented in detail by R. Hatcher

COST BASIS

- Basis for Cost and Schedule Estimates
  - Input from Vendors
  - Prior Experience
  - Similar tasks previously executed
  - Engineering Judgment
- Other aspects
  - Costs are essentially center -of-the-error bars
  - Areas of risk judged ; constraints noted
  - Contingency in the spreadsheet based on analysis of risks, general spread in quotes
- Cost & Schedule
  - Discussed in another area

SUMMARY

- TF, OH, PF1aU, PF1aL Power Loops redesigned to meet NSTX Upgrade requirements. Other circuits remain the same.
- System designed around space constraints in the facility.
- In TF loop, four additional branches added to meet the higher current of 130kA for 7.08 sec every 2400 sec. Loop designed to withstand the short circuit forces of nearly 4 times the existing level. Additional Power Cabling, and Current Limiting Reactors (CLR) are provided.
- OH Power Loop CLR value optimized based on PSCAD analysis.
- PF1aU & L ripple reduction reactors eliminated since these are not needed for the new coils having been built with higher inductance.
- New accurate fiber optic DCCTs (+/-150kA) provided to measure the TF current.
- Protection system upgraded to meet the new needs. Currently each circuit is protected from overcurrent, I^2*t, higher pulse duration and higher than permitted pulse period. In the new scheme force combination of current in coils are computed and protection accorded.
- Cost estimate is developed based on prior experience, similar tasks previously executed, vendor quotes, and engineering judgment.

CONCLUSION

- **FDR for Power System design meets the GRD requirements**
- **Cost & Schedule has been developed based on prior experience, similar tasks previously executed, vendor quotes, and engineering judgment. Design done keeping in view all constraints.**
- **Ready to proceed to Procurement & Installation.**

FCPC Rectifiers