NSTX

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Digital Coil Protection System

Ronald Hatcher

J. Lawson, R. Mozulay, and R. Woolley

and the NSTX Research Team

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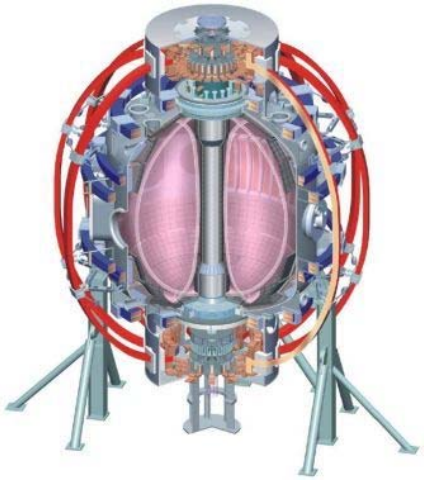

Background

- Operating envelope of NSTX_CSU significantly greater than that of NSTX
- Expansion due to increased magnetic field strength (coil currents), changes to device geometry, new coils systems, increased pulse length, and new operating scenarios
- Combined range of currents can result in forces, temperatures, and stresses to both coils and structures that significantly exceed NSTX design limits
- Access to full operating space would result in compromised structural integrity and in some cases catastrophic failure
- Mechanical solution is not feasible (complicated design, cost, schedule, and flexibility)

Background (cont.)

- Static methods could result in severe operation limitations (e.g., PF4-PF5 simultaneous operation)

- Project is determining critical set of values (forces, stresses, temperatures, combinations) that combined with their derivatives define the machine “state” with respect to machine integrity

Other Experiments

- DIII-D
  - Immediate “abort” (shutdown all power systems and short the OH coil) and “next shot prevention” protection
  - Thermally, the coils should be able to withstand the heat from one shot if cooling is lost during the shot (if the coil has totally cooled down from the previous shot)
  - Coil Monitoring
    - Ground Fault
    - Over current
    - Coil coolant flow
    - Coil coolant pressure
    - Coil outlet coolant temperature
    - Coil conductor temperature
    - B-coil (TF) bundle deflection
    - B-coil center post twist
    - B-coil pre-stress monitoring
  - Other (undocumented)

Other Experiments (cont.)

- C-Mod
  - Multiple non-integrated systems
  - Coil temperature monitoring
  - Real-time I^2t calculation and temperature modeling (microcontrollers)
  - OH force monitors (analog)
  - Over current protection
  - RF coupler protection
  - RF transmitter protection (in design phase)
  - Other (undocumented)

Design Basis

- DCPS will provide real-time protection to NSTX_CSU mechanical components
- DCPS algorithms will not only provide instantaneous protection but also in the “first derivative” sense
- The DCPS will not allow successive plasma attempts at a rate that exceeds the basic duty cycle of the NSTX_CSU (5 s / 1200 s = 0.4 %)
- Computing hardware shall be chosen with headroom for expansion
- Operation of the DCPS shall be fail safe. It will be impossible to run the machine with the DCPS faulted or in a powered off state
- The DCPS will, where reasonable, use “off the shelf” industry standard components

Design Basis (cont.)

- The DCPS will use redundancy, to the greatest extent possible, to increase reliability
- Any fault or failure on any DCPS unit will be considered genuine and cause a Level 1 fault
- Software shall be written in modern, structured programming language
- The DCPS software will include data archive and restore functionality
- The DCPS will be located indoors within a temperature controlled environment (heating and air conditioning) with a maximum ambient temperature of 24 ºC (FCPC junction area)

Benefits

- Easy reconfiguration – the DCPS algorithms and interlock limits can be easily changed in response to changing experimental requirements or changes in the state of the protected hardware
- The DCPS is capable of monitoring and interlocking a set intersecting/competing objectives with both unmatched accuracy and redundancy
- The DCPS algorithms can be exercised off-line for both post-shot evaluative analysis and for scenario development
- DCPS algorithms can provide data to other processes (psc, psrtc, etc.) that can be used to modify process behavior for fault and/or disruption avoidance
- Algorithms can be easily added for new hardware

Benefits (cont.)

- Self-check algorithms can continuously monitor system health
- The DCPS hardware and software will be capable of providing simultaneous protection on multiple timescales (coils-power-supplies control systems, forces, stresses and strains, thermal processes)

Functionality

- The set of limiting values and their derivatives define a “safe operating area” for the device. At any instant in time, the job of the DCPS is to ensure the integrity of the NSTX CSU mechanical structures via the following actions

1. Determine if any calculated value exceeds operating limit (initiate fault)
2. Determine if a power supply fault would result in conditions causing DCPS fault (initiate fault)
3. Determine if (given power supply response, present trajectory, etc.) any DCPS limit would be breached prior to next calculation time (initiate fault)
4. Predict a future time when it would be possible to attempt a plasma shot with a specified set of coil current envelopes
5. Determine a set of coil current envelopes allowable for a plasma attempt “right now
6. Compute and archive other quantities that over time can affect machine integrity because of fatigue

Functionality (cont)

7. Evaluate acceptability of potential operating scenarios (static and transient) for a given DCPS configuration

Design Requirements

- DCPS = real-time machine integrity determination and protection utilizing fast programmable digital system
- DCPS design will be fail-safe (redundancy)
- State continuously calculated on high-speed digital computer system and compared to pre-defined limits (like ISTP-001)
- DCPS will be easily reconfigurable via software (algorithms, state variables, and interlock values)
- Basic calculation interval similar to power supply response time (O(ms)) or less
- Provides protection via interface to existing Level 1 fault system

Design Requirements (cont.)

- The DCPS will include a “post-processor” to assist the operators in fault cause determination
- The DCPS shall include a software test suite that can be used to validate DCPS functionality (e.g., regression testing after changes)
- Scalable I/O for future expansion
- The DCPS will be a “standalone” system with respect to the laboratory network (security)
- Computing hardware to include extra capacity for future expansion (DCPS → MPS)

Current Design

Each DCPS unit will support 64 analog and up to 96 digital I/O channels

INPUTS

- Analog signals – currents, coolant flows, temperatures, pressures
- Digital signals – status bits from other systems
- All inputs will have over/under-voltage protection
- All inputs will be electrically isolated from the DCPS (e.g., opto-coupler)
- Digital Inputs: 5 V (TTL) or 10 – 32 V (high noise immunity)
- Analog Inputs: ±10 V
  - 4 kHz anti-aliasing filter
  - cable fault detection
- Reset Input: digital input (local pushbutton or remote electrical signal)
  - ACTIVE FAULT HAS PRECEDENCE

Current Design (cont.)

Outputs

- Currently only envision using one latched fault output fault signal per unit
- All outputs will utilize optical isolation to the outside world (e.g., opto-coupler)

Faults

- A protection interlock level is breached or will be breached prior to the next DCPS calculation time
- The combination of coil currents and temperatures are such that a power supply fault would move the system to a state corresponding to a DCPS faulted state
- Internal DCPS system integrity routines determine that there is a problem with the input data
- Internal DCPS self-check routines determine that program or internal data structures are corrupted
- Internal watchdog timer failure
- External watchdog timer failure

Algorithms

- PF coil supports
- Bus Bar stresses
- Outer leg insulation bond shear
- PF2 bracket and bolt stress
- PF3 bracket and weld stress
- Torques and stresses lid and spoke assembly (upper & lower)
- Vacuum vessel leg torque
- TF outer leg torque
- Forces on PF coils (single and combination)
- PF Coil moments (torque)
- Dome and PF rib stresses
- Coil thermal stresses
- Lid torque
- Leg and brace Hilti's™ (loads and moments)
- Knuckle clevis loads
- Ring loads and moments
- TF teeth torque
- TF joint bolts stresses
- Umbrella structure reinforcement (stress)
- OOP TF torque
- TF joint (forces, torques)
- TF coil torsional shear stress
- OH fatigue (long term)
- TF shear forces between TF turns, insulation, and insulating crown
- Coil temperatures (i^2t heating)

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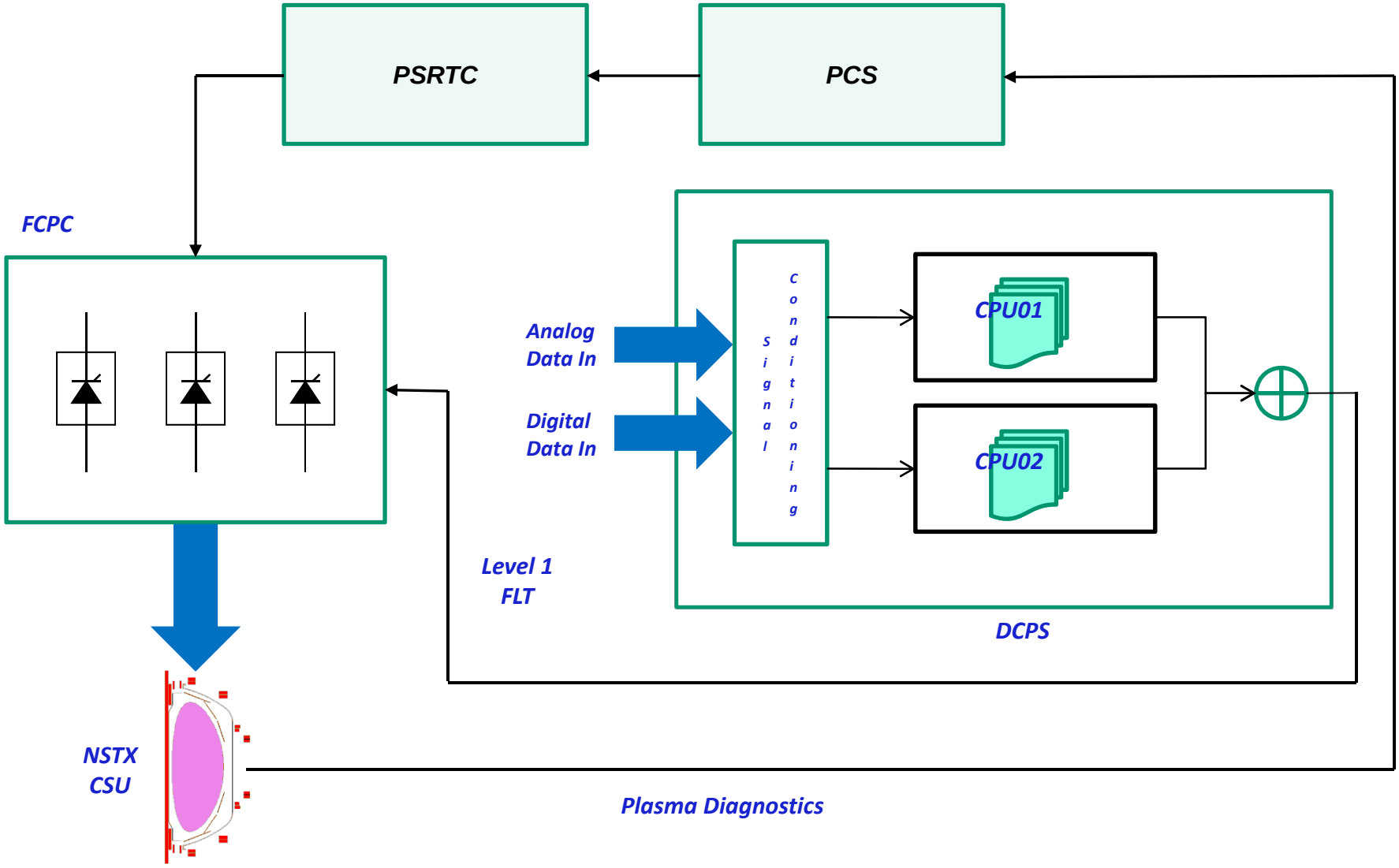
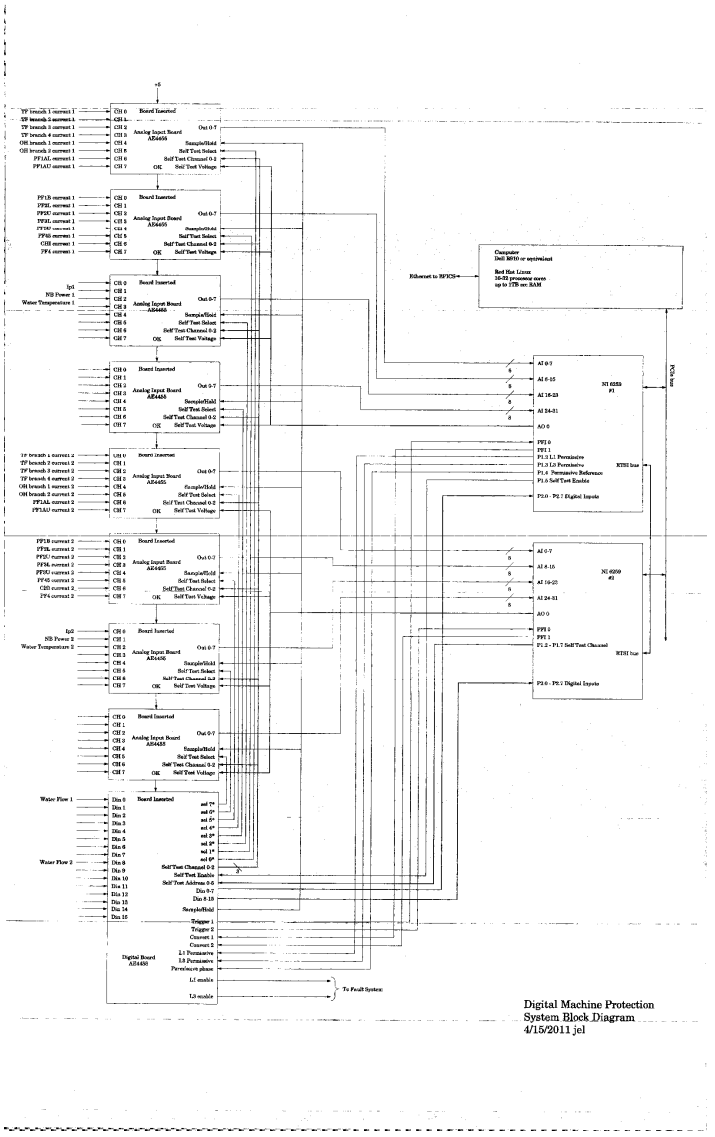
Block Diagram with DCPS



DCPS Hardwaer Block Diagram (1/2)

- Eight, 8-channel analog input boards
  - Analog inputs with 5-pole, 4 kHz input filter and self-test feature
- Digital input board
- 2 – National Instruments 6259 1.25 MS/s DAQ
- I/O Board
- 8 Channel Analog Input Board with 5-pole, 4 kHz input filter and self-test feature
- Dell PowerEdge R910



Schedule

- Successful CDR completed 3/2011
  - Chit resolution ongoing (most resolved, one meeting to go)
- Systems code is under development (Woolley) with beta version expected in June
  - Will be used to exercise DCPS algorithms on NSTX and NSTX CSU configurations during next two run periods
- System drawings for preliminary design complete and under review
- PDR scheduled for June (tentative date 6/17)
  - One external reviewer commitment (try for one more)
- FDR to follow in 2012