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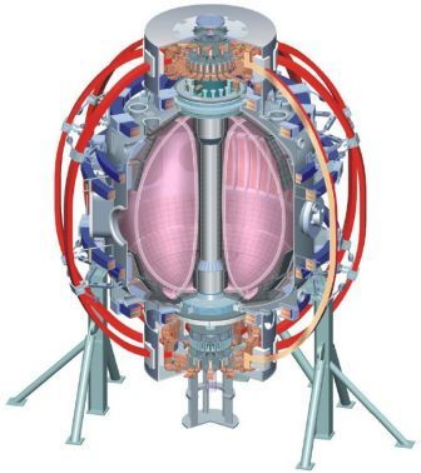
NSTX Upgrade Project
Conceptual Design Review
LSB, B318
October 28-29, 2009



PWR SYSTEM UPGRADE FOR NEW CENTER STACK

- REQUIREMENTS
- TF : 129.8 kA, 1kV, ESW 7.08 sec every 2400 sec (7.05kA rms) ;
- OH : 24kA, ESW .9 sec every 2400 sec ; 8kV

- PF : Existing configuration will meet requirements

- CONSTRAINTS:
- Constraints analyzed to project realistic estimate
  - NSTX machine is located in NTC - is small in area.
  - Constrained space in the basement of NTC
  - FCPC Building has limited space & equipment is virtually crammed inside. No basement in this building.
  - Thus real estate availability is very limited and design of upgrades has to meet these limitations
  - d) TF has now four parallels. Thus short circuit current about 250kA. Upgrade dictates doubling parallels - short circuit current also gets doubled – the forces are four times more. Hence power loop components require appropriate upgrade. Also additional protective measures are required.

TF POWER LOOP DESIGN

- **Four additional PARALLELS of Transrex power supplies to be provided to existing four parallels**
- **Each parallel - two 1 kV Transrex power supply sections in series.**
  - **CLRs will be connected between the supplies**
  - **One section of the supply will be used as a Diode**
- **Existing four SDS of TF with additional parallel supplies will be used.**
  - **two parallels to be fed via each switch.**
- **Four more DC reactors (270uH) to be used in the additional 4 parallels.**
  - **Since upgraded OH circuit needs reactors of higher inductance, the existing 270uH OH CLRs will be reconnected in the TF Circuit.**
- **To install reactors in TF wing**
  - **(1) Remove PF1a Ripple reduction Reactors & store; and**
  - **(2) Remove four CICADA Racks in the middle of isle.**

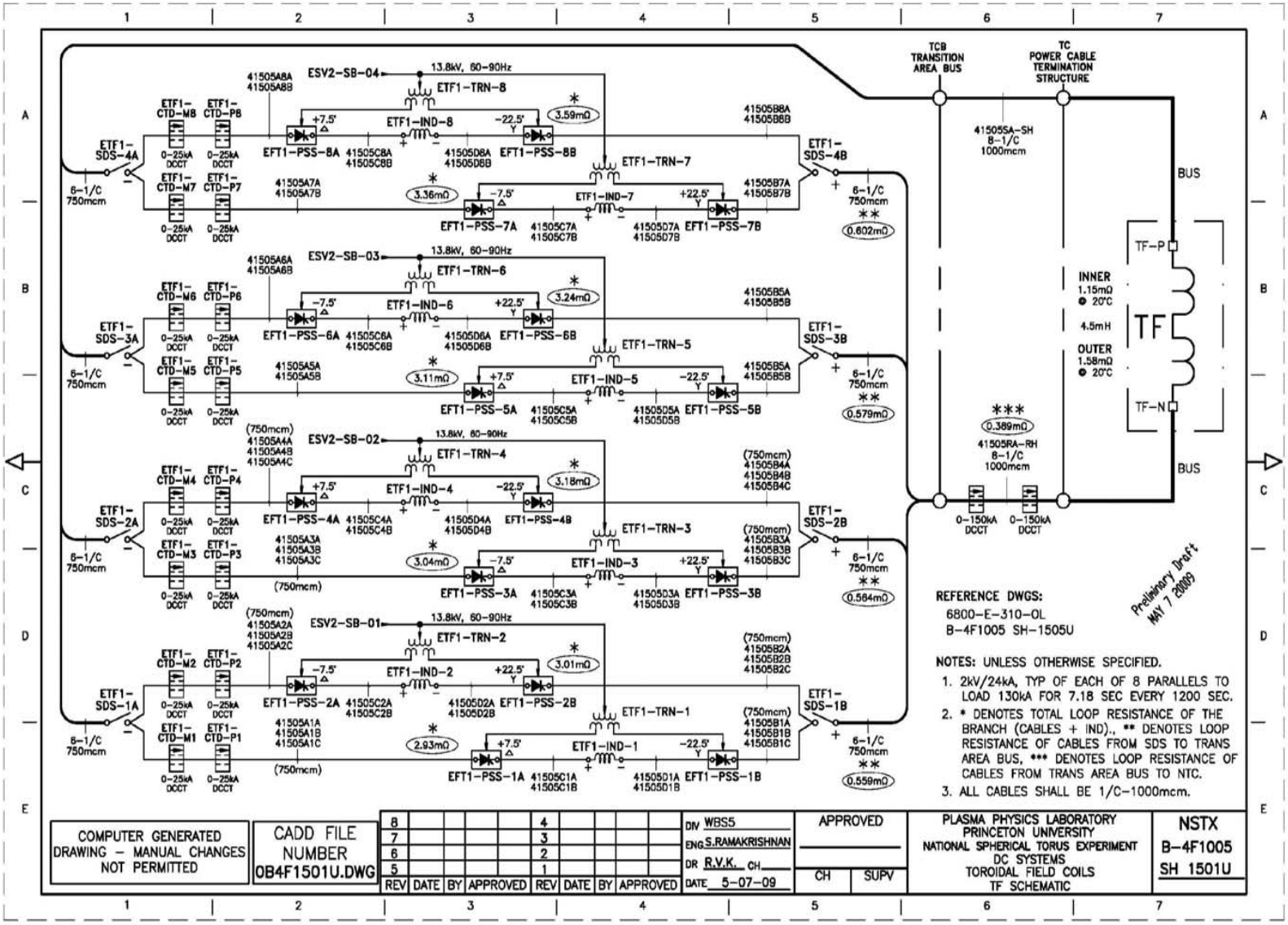
TF POWER LOOP DESIGN – Contd.

- **DCCTs**
  - Existing eight DCCTs will be repositioned to detect current in each of the eight parallels
  - Eight additional DCCTs will be purchased and installed
  - Two new DCCTs to detect total TF Coil Current

- **CABLING**
  - Reconnect existing cabling as needed.
  - Install additional power cabling within FCPC - nearly 6000 feet of 1000mcm 5kV power cables. Limited space makes bus installation difficult
  - Reconnect existing power cabling in Transition Area (TA) - in TFTR Test Cell Basement- to NSTX Test Cell for TF use.
  - Provide Control Cabling as needed

- **Modify Power Cable Termination Structure (PCTS) for TF to handle fault currents & to accept 3 more power cables/pole.**

TF CIRCUIT – 129.8kA, 1kV (8 parallels)



OH PWR. LOOP DESIGN & PF PWR. LOOP DESIGN BASIS

EXISTING OH PWR LOOP DESIGN:

- 6kV Anti-parallel configuration
- 24kA for 0.4 seconds every 600 seconds

UPGRADE - OH PWR LOOP DESIGN:

- 8kV Anti-parallel configuration
- 24kA for 0.9 sec every 2400 seconds

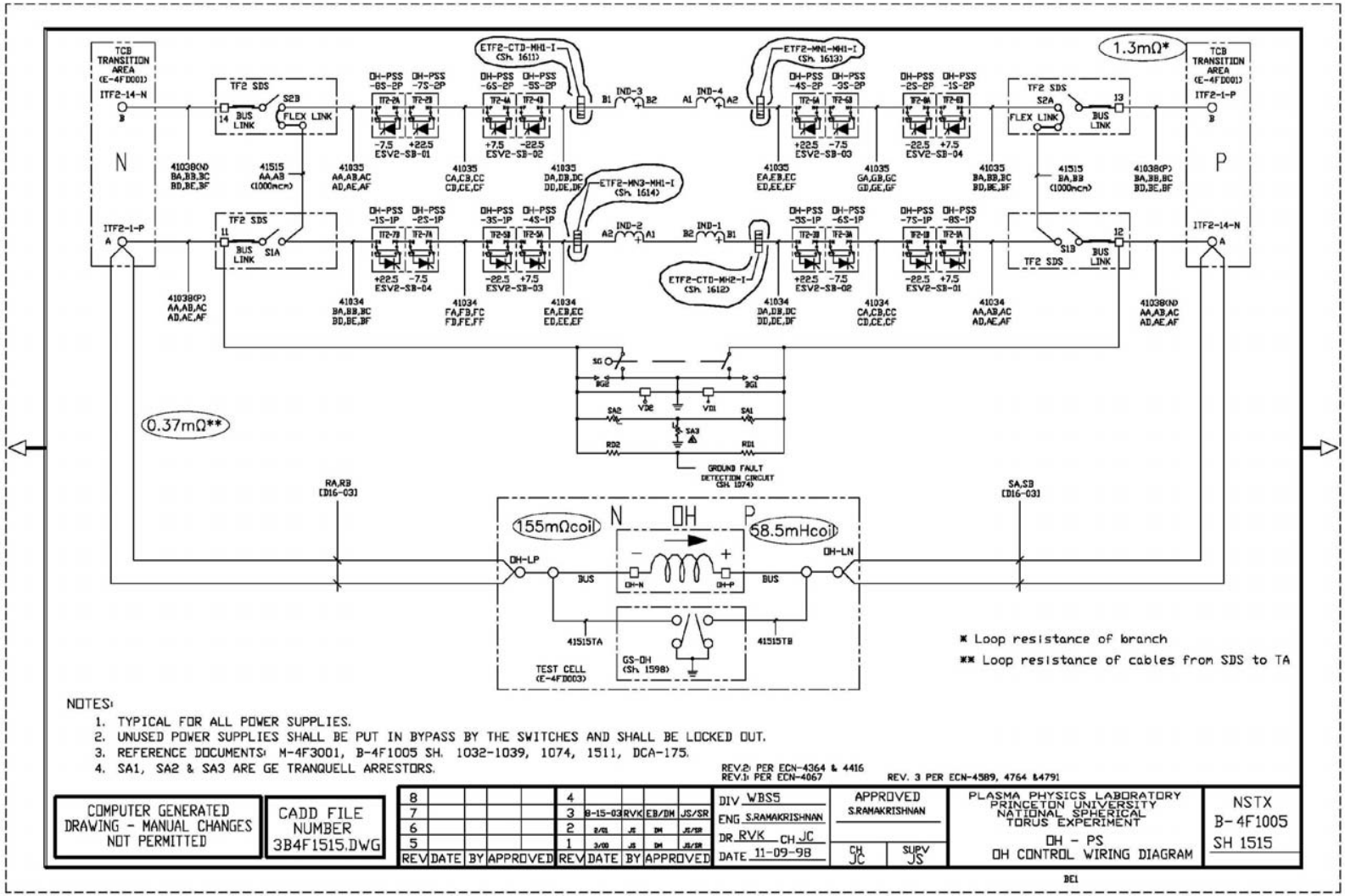
Work Required

- 2kV installed standby is available in each of the anti-parallel branches. Hence these supplies will be switched into the circuit.
- The DC CLR values will be optimized to the new requirement based on PSCAD analysis. Thus new reactors of the required values will be purchased and installed.
- All the other equipment and cabling in the power loop will be used AS IS

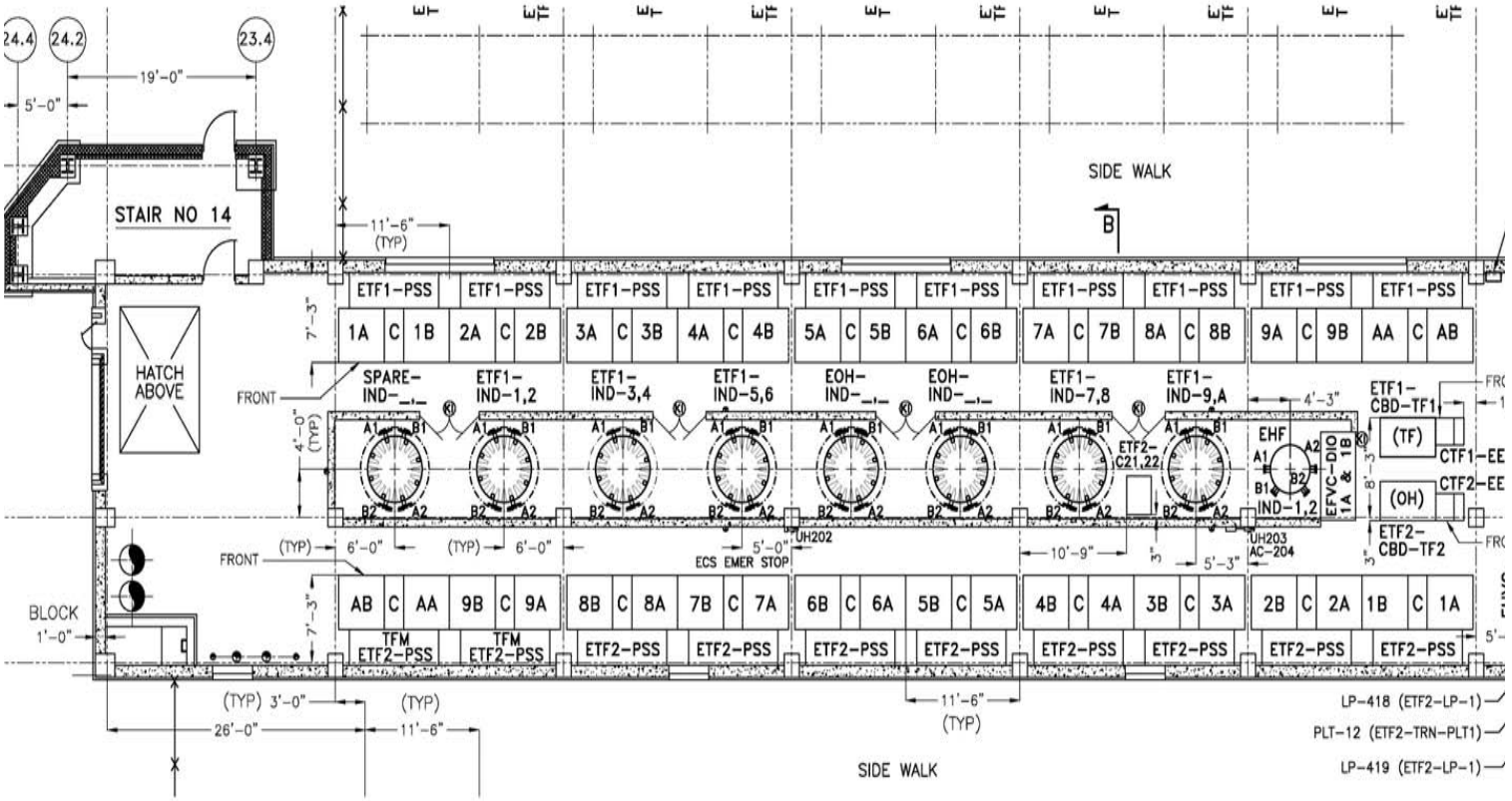
PF DESIGN:

- Existing PF circuits will be used AS IS for the upgrade except for PF1a wherein the ripple reduction reactors will be eliminated.

OH CIRCUIT – ANTI-PARALLEL 8kV;+/-24kA



FCPC BLDG. TF WING - EQUIPMENT LAYOUT



CONTROL & PROTECTION

- CONTROLS
  - Hardwired Controls will be upgraded – proposing to use PLC
  - Firing Generator (FG) & Fault Detector (FD) will be replaced

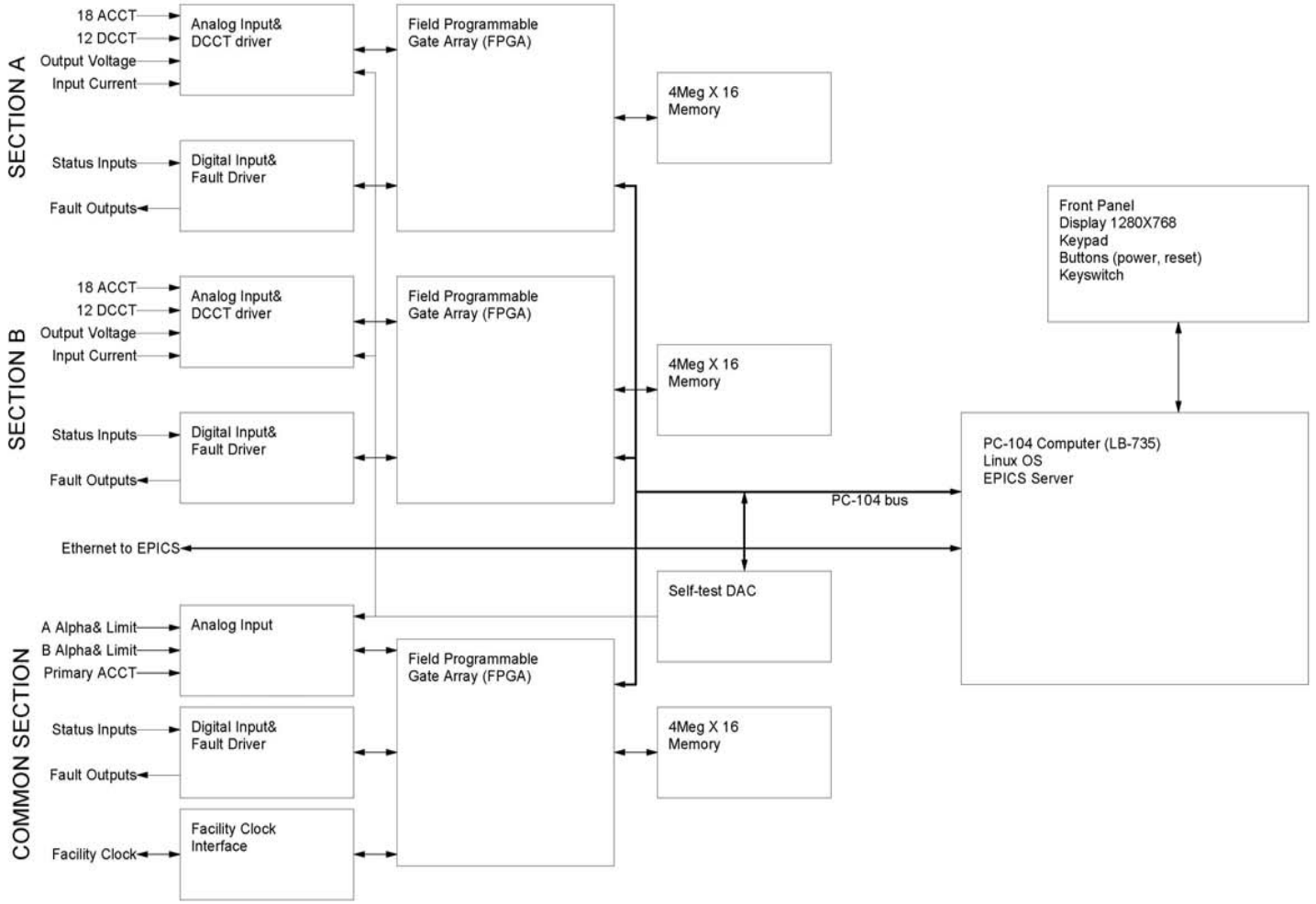
- CIRCUIT PROTECTION
  - Old RIS will be replaced with Analog Coil Protection Units (ACPs)

- RECTIFIER PROTECTION
  - ACCT, DCCT & PT signals along with other interlocks will be processed in the FD. See Block diagram.
  - Fault Detector (FD) in Rectifiers will be replaced
    - To upgrade the device for faster action
    - Enhance the reliability
    - Eliminate the CICADA rack (Transformer alarms to CICADA not needed)
    - Use State of the Art Components
    - **EPICS Compatibility**
      - The fault detector will be able to interface with the existing data acquisition system either as an EPICS server or as an EPICS IOC.
    - **Configuration Files**
      - All operational settings will be saved in one data file in FD. This will allow for easy setting of operational profiles.
    - **Removable Storage**
      - The fault detector will have some form of removable storage
    - **Real World Values**
      - All monitored points and limit settings must be in scaled engineering units
  - FD will generate Level 1, 2, 3 faults to trip.

- Machine Protection System (MPS):
  - MPS will be designed for protecting the machine support system.
    - Algorithms will be developed and implemented
    - Hardware will be designed & installed
    - Software will be written to meet the requirements
    - System will be tested.

FD BLOCK DIAGRAM

Ed Lawson



COST BASIS

- Basis for Cost and Schedule Estimates
  - Input from Vendors
  - Prior Experience
  - Similar tasks previously executed
  - Engineering Judgment
- Other aspects
  - Costs are essentially center -of-the-error bars
  - Areas of risk judged ; constraints noted
  - Contingency in the spreadsheet based on analysis of risks, general spread in quotes
- Cost & Schedule
  - Discussed in another area